P.M.G. RESEARCH LABORATORIES -

LABORATORY NOTE

FS-1

A Decadic Pulse Counter Employing a Novel Sequence of States

1. Introduction:

In the course of development of equipment in the Frequency Standards Division a need arose for decade pulse counters possessing certain characteristics. These are:

(a) High fan-out carry capability.

(b) Decodability, such that no decimal output line from a decoder can possibly carry false pulses caused by non-zero switching delays or other non-ideal operations.

(c) Encodability, such that any combination of states may be set into the counter. In particular, the states corresponding to count '0' must be settable by operating a single control line - even, if necessary, while the input pulse train continues.

The counter to be described employs four flip-flops and a number of two-input gates to implement the desired sequence of count states. The sequence is known as Decade Sequence 23.8.67.

2. Design Choices:

The design is based upon HIGH true NAND logic. The printed circuit board, RPC 281, has been laid out to accept Texas Instruments SN74N series TTL integrated circuits.

To minimise pulse delay from input to output of the counter, the sequence is designed for synchronous edge-triggering.

To aid decodability the sequence of states involves no more than one flip-flop changing state when advancing the count by one. This is, of course, only possible when the closed sequence consists of an even number of steps. It also implies that the code produced by the sequence must be an unweighted code.

To aid encodability, the set of flip-flop states corresponding to count '0' should consist of 0000 or 1111. For reasons which will become apparent the set 1111 was chosen.

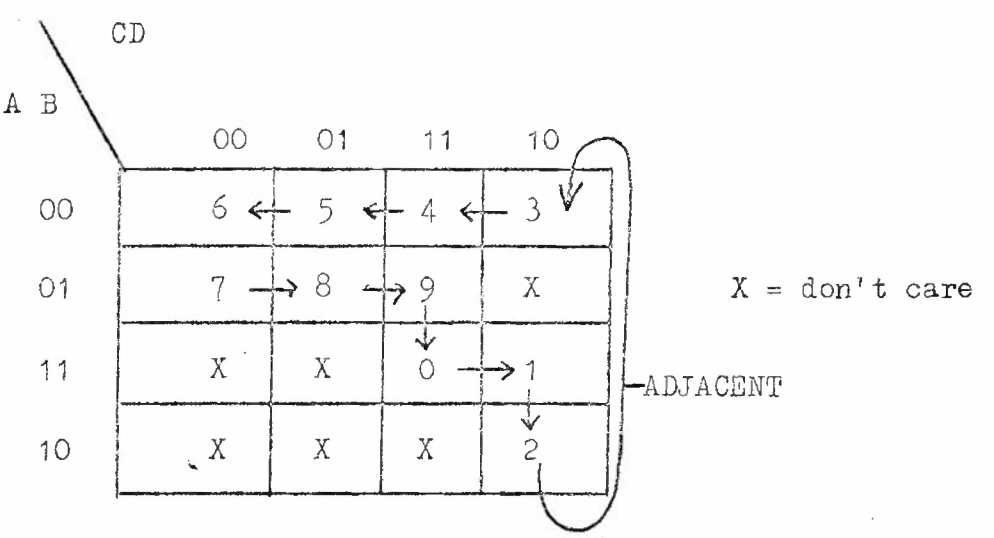
The Type 'D' flip-flop was chosen since its CLEAR and PRESET inputs take precedence over clock signals, allowing encoding to take place while the input pulse train continues.

3. Practical Design:

The final design is shown on the logic diagram. The required gating was decided by the use of Karnaugh Maps. To aid understanding of the waveforms obtained, a truth table is also given. As well, a cyclic state-sequence indicates the paths of entry into the desired sequence from undesired commencement states.

The Karnaugh Map is arranged in such a way that if, in a sequence of states, movement from one set of states to the next requires only vertical or horizontal movement from one square to a neighbouring square, then only one variable changes at each step. The two vertical edges of the map can be regarded as being adjacent in the above sense, as can the two horizontal edges. Thus the map can be visualised as consisting of the unbroken surface of a doughnut.

The first Karnaugh Map below shows the path followed by the count sequence adopted.



The following features are apparent:

(i) The lower half of the map is largely avoided. This effectively prevents the A output being loaded by sequence gating.

(ii) Feature (i) leads to the choice of A to provide the maximum fan-out carry output.

(iii) The only 0 to 1 transition for the A flip-flop occurs at the step from natural BCD number 7 to number 15. This decides the choice of representation of count '0' by the combination of states 1111.

(iv) The set of states corresponding to natural BCD number 6 is avoided. This avoidance is based upon a practical consideration. By so doing the use of three-input gates is avoided and the number of two-input gates required is kept to a minimum without compromising the other desired features of the counter.

The minimum gating necessary to ensure that the sequence is followed is obtained in the conventional way be setting up a map for each 'D' input and grouping to obtain the appropriate minterms. We make use of the fact that the Type 'D' flip-flop has only one data input and its output equals the 'D' input one bit-time earlier. The maps and resulting equations are shown below. The terms in the equations are also shown on the logic diagram. The logical implementation of the equations is shown below.

It can be observed here that when using a counter employing a natural BCD counting code, the flip-flop generating the carry output is generally designated D. The natural BCD or 1248 code is a weighted code, with A being the least significant digit and D the most significant. The sequence described here generates an unweighted code and thus the flip-flop generating the carry output could equally well have been called A, B, C or D. The choice of A is purely a function of the labelling of the map showing the sequence of states.

AB \ CD	00	01	11	10
00	6	5	4	3
01	7	8	9	X
11	X	X	0	1
10	X	X	X	2

Count Sequence

AB \ CD	00	01	11	10
00	0	0	1	1
01	1	1	1	X
11	X	X	0	0
10	X	X	X	0

Flip-Flop D

$D_D = \overline{A}.B + \overline{A}.C$

AB \ CD	00	01	11	10
00	0	0	0	1
01	0	1	1	X
11	X	X	1	1
10	X	X	X	1

Flip-Flop C

$C_D = B.D + C.\overline{D}$

AB \ CD	00	01	11	10
00	1	0	0	0
01	1	1	1	X
11	X	X	1	0
10	X	X	X	0

Flip-Flop B

$B_D = \overline{C}.\overline{D}. + B.D.$

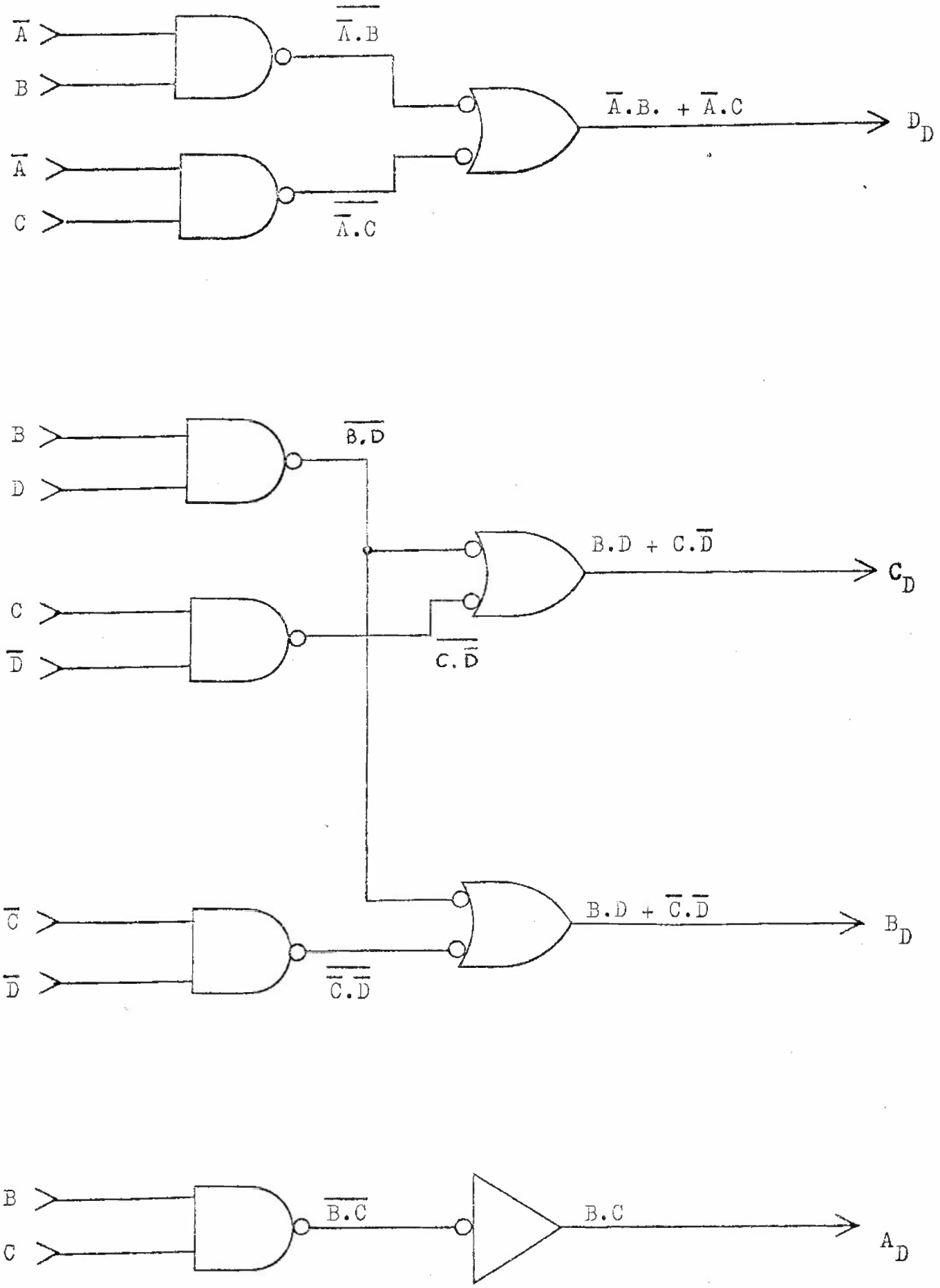
AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	1	X
11	X	X	1	1
10	X	X	X	0

Flip-Flop A

$A_D = B.C.$

AB \ CD	00	01	11	10
00				
01				X
11	X	X		
10	X	X	X	

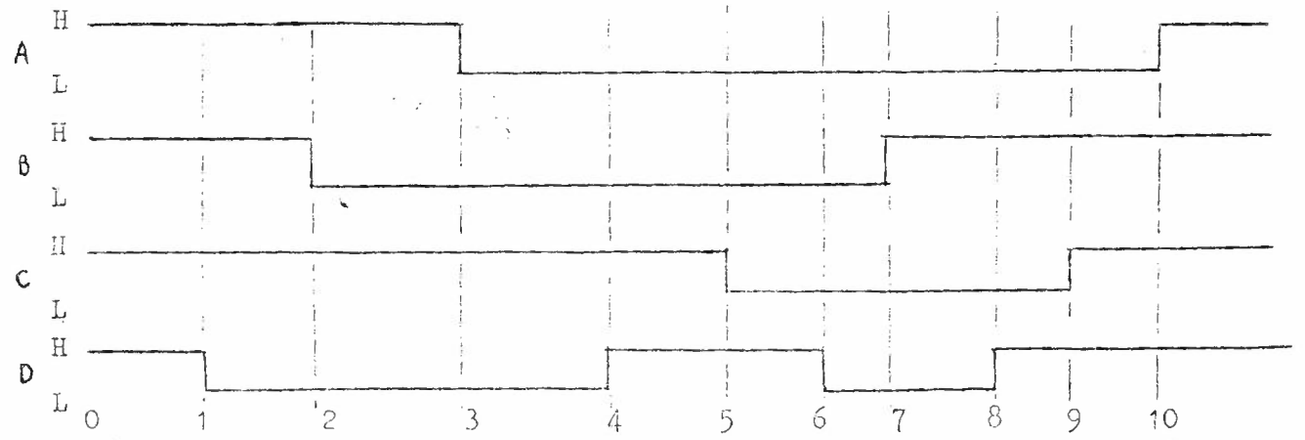
Paths From Undesired States to Desired States in the Sequence.



LOGICAL IMPLEMENTATION OF GATING EQUATIONS

A truth table, including the undesired commencement sets of states, is shown below:

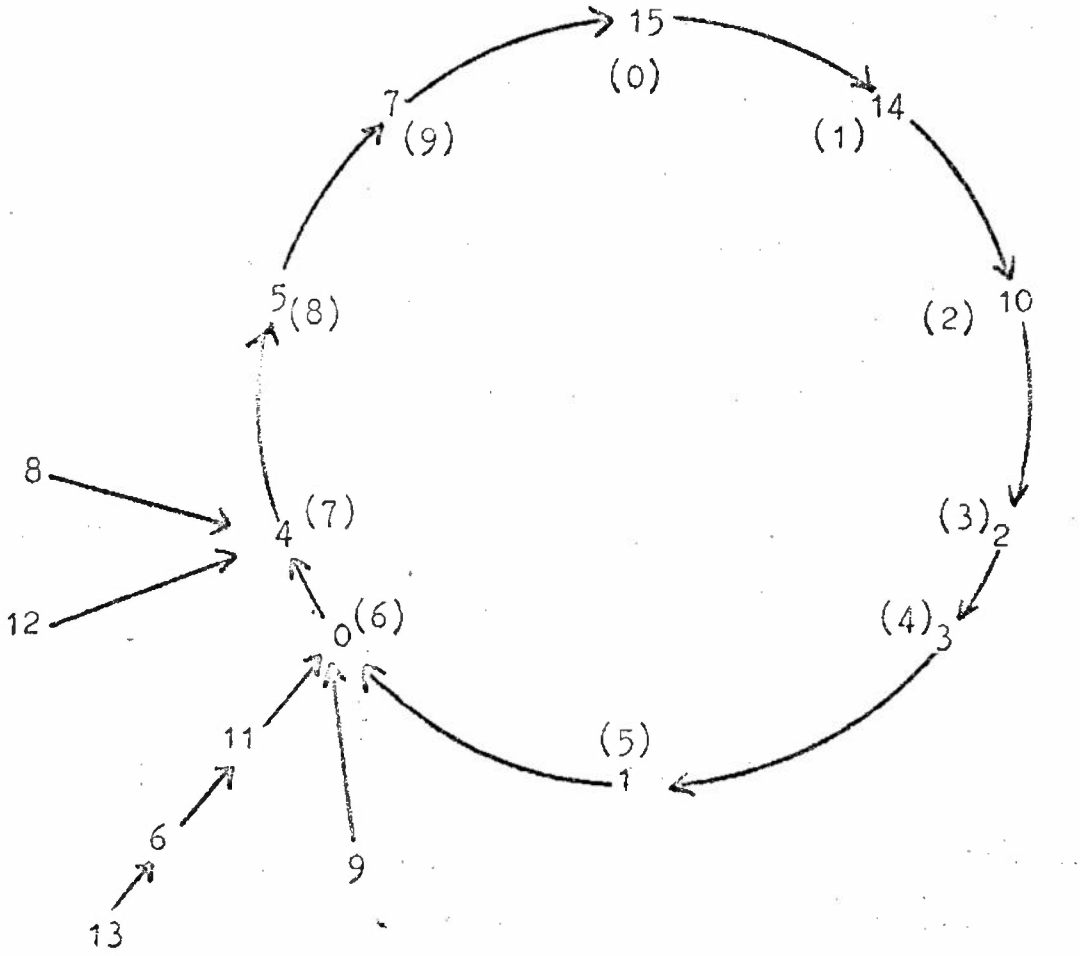
COUNT	A	B	C	D	NATURAL BCD NUMBER
0	1	1	1	1	15
1	1	1	1	0	14
2	1	0	1	0	10
3	0	0	1	0	2
4	0	0	1	1	3
5	0	0	0	1	1
6	0	0	0	0	0
7	0	1	0	0	4
8	0	1	0	1	5
9	0	1	1	1	7
UNDESIRED SETS OF STATES	0	1	1	0	6
	1	1	0	0	12
	1	1	0	1	13
	1	0	0	0	8
	1	0	0	1	9
	1	0	1	1	11



WAVEFORMS FOR DECADE SEQUENCE 23.8.67

The values of A, B, C and D for each of the undesired sets of states can be substituted into the equations and the values of A_D, B_D, C_D and D_D obtained. These values will be clocked into A, B, C and D respectively by the next clock pulse. If the new ABCD is a desired set of states, the desired sequence will then progress normally with each clock pulse advancing the count by one. If the new ABCD is another undesired set of states a further step is needed to reach a desired set of states in the sequence.

The diagram below shows the procession of cyclic sets of states together with entry paths from the undesired sets of states. Each set of states is represented by its natural BCD equivalent, with the appropriate count number shown in brackets.



4. Summary:

The circuit described performs the following functions:

(a) Starting in random condition, it will automatically be driven into the desired sequence of states by the input clock pulses.

(b) By holding the GATE CARRY O/P line HIGH, two separate outputs each capable of driving 10 loads are made available. Alternatively the A line can be used as a 10 load direct output and the GATED CARRY O/P can be gated on or off according to the state of a control signal on the GATE CARRY O/P line.

(c) By driving the ENABLE ENCODE line LOW, the states existing on the ENCODE A, B, C and D lines are set into their respective flip-flops. If the ENCODE A, B, C and D lines are permanently held HIGH, resetting the counter to '0' is simply accomplished by momentarily driving the ENABLE ENCODE line LOW. These functions can be carried out regardless of the state of the clock line.

(d) Since in proceeding from one set of states to the next only one flip-flop changes state, unambiguous decoding with no possibility of false pulses can be performed using printed circuit card RPC 282A.

(e) Since only two levels of gating are used in the sequence gating and the flip-flops are clocked synchronously, the counter will operate up to a clock rate very nearly as high as that of a Type 'D' flip-flop alone.

5. Acknowledgement:

I enjoyed friendly argument with G.M. Willis during the course of this work.

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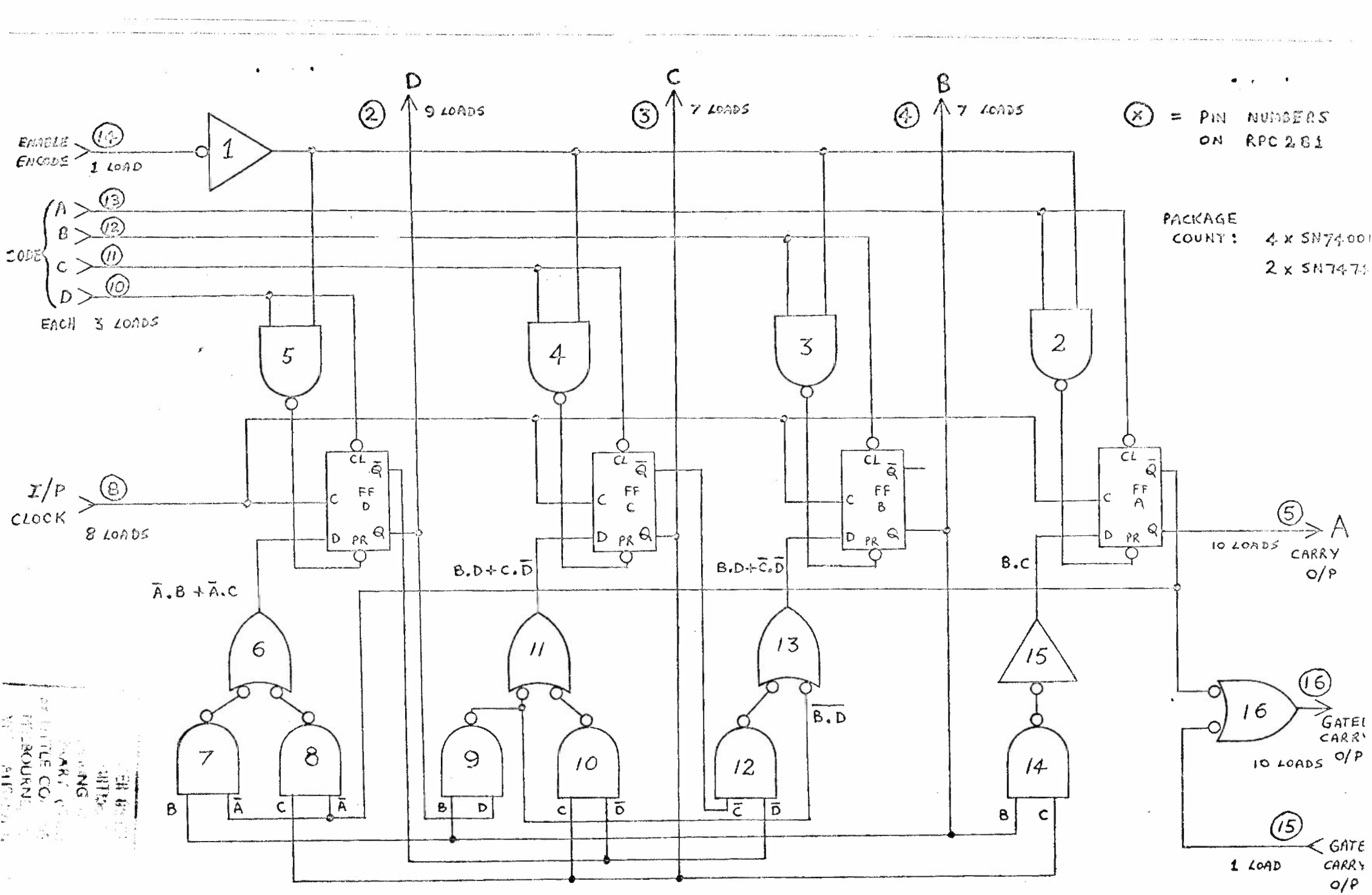

LOGIC DIAGRAM FOR DECADE SEQUENCE 23.8.67