# Research Laboratories

Report Number 6914

**Single Channel P.C.M. Codecs**

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ABSTRACT

This report collates the findings of several people who have worked on single channel PCM codecs over a period of about four years. The report gives descriptions of the various types of codecs built, and records some measurements taken on them.

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(Sgd.) R. SMITH
for Director, Research

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# SINGLE CHANNEL PCM CODECS

## 1. INTRODUCTION

Up to the present time the main use for single channel PCM codecs (coder-decoder) has been for encoding and decoding information in order to drop and insert a single channel on one PCM time slot. With the extension of PCM into the telephone network, and the possibility of carrying out the coding process at or near the subscriber, the need arose for investigation of single channel PCM codecs. This report records the investigation into various types of single channel PCM codecs. It should be noted that all the codecs described in this report use the A-law companding characteristic. However, some information on the principles of Mu-law codecs is also given.

## 2. C.C.I.T.T. RECOMMENDATIONS FOR PCM CODECS

The C.C.I.T.T. recommendations for characteristics and performance of PCM codecs (Ref. 1) are now well established. Although the recommendations refer to group codecs, almost all of the recommendations can be applied to single channel codecs. Recommendations such as interchannel crosstalk, interference from signalling etc. are not applicable to single channel codecs. This report uses C.C.I.T.T. recommendations (G.711 and G.712) as a basis for evaluating all aspects of single channel PCM codecs.

2.1 Companding Laws. Recommendations for companding laws are the use of the Mu-law for 24 channel 1.544 Mbit/sec PCM systems, and the A-law for 2.048 Mbit/sec systems.

Both A-law and Mu-law systems use 8 digits to represent an input amplitude. In serial form the first digit represents the sign of the input amplitude; the next three digits, called the exponent bits, determine in which segment of the characteristic the input amplitude lies, giving a possible 16 segments. The last four digits, called the Mantissa bits, locate the position of the input amplitude within the segment. Each segment can therefore be divided into 16 steps. The step size within segment 2 is double the step size within segment 1. The step size within segment 3 is double the step size within segment 2, and so on. Segment 1 corresponds to the lowest level analog signals.

In the A-law the four segments about AC zero have the same step size, and are combined into one segment, giving a total of 13 segments (12 with 16 steps and 1 with 64 steps).

In the Mu-law the two segments about AC zero have the same step size, and are combined into one segment, giving a total of 15 segments (14 with 16 steps and 1 larger segment). The first segment has 31 parts because the first step is split about AC zero. See fig. 2.

2.2 A/D Conversion. Figures 1 and 3 show the recommended A/D transfer characteristics for the A-Law. Note in figure 1 that about AC zero a step "rises" (termed mid-riser coding). Table 1 shows some steps in the A-law coding process. Note that a 12 bit binary code is required to express all the coder decision amplitudes. It can also be seen that the mantissa bits in the companded digital code (bracketed), can be extracted directly from selected positions (also

bracketed) in the 12 bit binary code. Table 2 shows this in a simpler format.

Figures 2 and 4 show the recommended A/D transfer characteristics for the Mu-law. Note in figure 2 that about AC zero the first level "steps" (termed midstep coding). Table 2 shows some steps in the Mu-law coding process. Note that a 14 bit binary code is required to express all the coder decision amplitudes.

2.3 D/A Conversion. It has been shown (Ref. 2), that for given coder decision levels, the locally optimal (minimum mean squared error) placement of the output levels lies midway between adjacent coder decision levels. Referring to table 1 it can be seen that this is achieved in the A-law by shifting the output level a half step up in the compressed signal domain. This necessitates the addition of a fixed half L.S.B. (Least Significant Bit) offset, to the decoded analog output. One way of achieving this is to make the decoder capacity one bit larger than the encoder, and fix the L.S.B. of the decoder to a "1". Note that a 13 bit binary code is required to express all the decoder output amplitudes.

In the Mu-law the first step is split about AC zero, placing the optimal output level for the first step at 0 (see table 3), and placing subsequent output levels for Segment 1 at even numbered output levels. In all other segments the output levels are odd numbered. Note that a 14 bit binary code is required to express all the decoder output amplitudes and the binary code does not follow any easily recognisable pattern as does the code for the A-law. Further study is required on the Mu-law.

2.4 Overload Level. The recommended overload level for PCM coders is +3dBm0. To overcome the problem of the different overload levels of the various coders, a variable gain amplifier was inserted at the analog input of each coder during testing. The gain of the amplifier was adjusted separately for each coder to give each coder an overload level of +3dBm0. The following method was used to adjust the overload level.

(i) A variable DC voltage was connected to the input of the codec (without amplifier or LP filter).

(ii) The DC voltage was increased until the occurrence of the largest pulse amplitude modulated sample at the decoder output.

(iii) The amplitude of the DC voltage was then recorded.

(iv) The variable gain amplifier and LP filter were then connected to the codec input, and a 1 kHz sinewave applied to the input of the amplifier and LP filter.

(v) The gain of the amplifier was then adjusted to give a peak sinewave level at the codec input equivalent to that recorded in (iii). The nominal input level is then achieved by reducing the input level by 3dB.

## 3. DESCRIPTIONS OF CODECS BUILT

3.1 A.W.A. 1395/1396 Codec. This integrated circuit codec has been designed and produced by A.W.A. as a commercial product. The AWM1395 is an A-law PCM decoder. To use the AWM1395 as a complete PCM decoder, an operational amplifier and a LP filter are required. Circuit 1 shows a PCM decoder utilising the AWM1395. The AWM1396 is a successive approximation register, which is used in conjunction with the AWM1395 to form a PCM encoder. A comparator sample and hold, and LP filter are also required to form a complete encoder. Circuit 2 shows a PCM encoder utilising the AWM1395 and AWM1396. The AWM1395 does not provide for the fixed half L.S.B. offset as described in section 2.3 Figure 6 gives the waveforms for the AWM1396.

3.2 Codecs with Successive Approximation Control Logic. All the codecs described in this report use the successive approximation technique for A/D conversion. Successive approximation A/D converters operate by comparing an unknown analog input against a time-dependent feedback voltage derived from a D/A converter. Conversion proceeds one bit at a time with the sign bit generated first. For the first iteration the sign bit is made high with all the remaining bits low. This number is fed to the D/A converter and a comparison is made between the resulting output of the D/A converter and the sampled incoming analog signal. The comparator determines which of its 2 inputs is larger, and a "1" or a "0" is sent to the control logic to set the state of the sign bit. At the same time the next M.S.B. (Most Significant Bit) is made high ready for the next iteration. The conversion proceeds one bit at a time up to the L.S.B., when the output of the D/A converter should match the sampled incoming analog signal as closely as the L.S.B. of the D/A converter will allow.

Circuit 3 shows the successive approximation control logic used for the encoders described in sections 3.4 and 3.5 and incorporates an Am2503 successive approximation register in the circuitry. Waveforms for circuit 3 are shown in fig. 5.

The Am2503 takes nine clock periods to achieve conversion. Seven clock periods have been allowed before conversion for the sample and hold circuitry to take a sample of the incoming analog signals. The sampling time could be reduced by using faster sample and hold circuitry. When the S.B. (Sign Bit) is a "1", the data fed into the register is inverted via an Exclusive On gate. This facility is required as part of the PCM code conversion process of inverting the code when the S.B. is an "0".

Comparison of the waveforms of figures 5 and 6 show that conversion only takes eight clock periods for the AWM1396, as against nine clock periods for the Am2503. This means that the AWM1396 can use a sample and hold waveform with one less clock period hold time than the Am2503. However, examination of the waveforms of figure 6 shows that, under certain conditions, the logic states of successive output bits could alternate at each half clock period. The analog output level of the D/A converter could therefore change at each half clock period. This places greater restrictions on the settling time of the D/A converter than in the case of the AM2503. Referring to fig. 5, the logic states of successive output bits can only change state at each full clock period. The AWM1396 therefore has to be used with a D/A converter having a settling time of at least half that of a D/A converter used with the Am2503 for optimum performance at maximum sampling frequencies.

3.2.1 Zeltex linear D/A Modules with Digital Expansion. This codec utilises a 12 bit Zeltex linear D/A converter module together with digital expansion as a PCM decoder. The expander converts the PCM code into a linear code. The encoder makes use of a decoder, as just outlined, together with the successive approximation logic as per circuit 3. For descriptive purposes, only the decoder will be considered, as the circuitry is virtually identical for both encoder and decoder.

A circuit of the digital expander is shown in circuit 4. The heart of the expander consists of the two 8 bit position scalers B2 and D1. Under control of the three exponent bits, the four mantissa bits are shifted up or down the 12 bit linear code. A representation of the mechanism employed is shown in table 2. Or gates A1, together with inverter A2, ensure that the exponent bits addressing B2 are the same for the two halves of segment 1, and thus forcing B2 to position the mantissa bits to the same point in the linear code. For the two halves of segment 1 the fifth L.S.B. of the linear code is connected, via B2, to A1(11). A1(11) is a "0" for the first half of segment 1, and a "1" for the second half of segment 1. This was included so that the linear decoder could distinguish between the two halves of segment 1. Provision of a fixed extra L.S.B., as described in section 2.3, has not been provided for on the digital expander as shown in circuit 4. However, the extra L.S.B. could be provided on all segments except segment 1, by changing 16 of B2 from an "0" to a "1". To utilise the extra L.S.B. in segment 1 a 13 bit decoder is required.

The Zeltex 12 bit linear D/A converter is supplied as a module, and only requires a latch on the digital inputs to function as a complete linear decoder. A circuit of the complete decoder is shown in circuit 5.

3.2.2 Non linear Codec. This codec uses a 7 bit linear D/A converter, together with a 7 step analog attenuator, as a complete PCM decoder. A circuit of the decoder is shown in circuit 6. The encoder uses a decoder, as just outlined, together with the successive approximation logic as per circuit 3. The L.S.B. of the linear D/A converter section of the decoder is a fixed offset, and is added for reasons described in section 2.3. When the decoder is used with the successive approximation circuitry as an encoder, the L.S.B. used for the decoder must be disconnected. For descriptive purposes, only the decoder will be considered, as the circuitry is virtually identical for both encoder and decoder.

Referring to circuit 6, the PCM code is applied via latches A1 and A2. A facility for inverting the code is provided after the latches. Exclusive Or gates B1 and B2 invert the modified PCM code into the linear D/A converter section when the sign bit is a "1". The state of the sign bit controls the M.S.B. of the linear D/A converter section. The second M.S.B. is controlled by A3(1), which is an "0" for the first half of segment 1 and a "1" for the second half of segment 1 and all other segments. The next four linear D/A converter section bits are controlled by the mantissa bits.

Transistors TR1 and TR6 switch current from the +10v reference voltage, supplied by C1, through the resistor network R1 to R6, under control of the input digital code. The transistors are operating in an inverted mode condition which gives a very low saturation voltage

(approx. 10mv). The current through R7 supplies the fixed L.S.B. offset required for the extra L.S.B. as described in section 2.3.

Resistors R8 and R9 form a voltage divider making the voltage on the positive input to C2 +5v. Thus the negative input to C2 is set to +5v. The current through R10 is therefore fixed at 500μA. The only return part for this current is through R11 and/or the resistor network. As the parallel combinations of the resister network varies under control of the digital input code, the current through these resistors, and thus through R11 will vary. The variation in the current through R11 causes the voltage across R11, and therefore the voltage at the output of C2 to vary. R11 and/or R7 may have to be trimmed to compensate for the bias current of C2.

The output of C2 is applied to an R/2R ladder network, which attenuates the output of C2 by half for each step down the ladder. The outputs of the R/2R ladder network are connected to the inputs of an 8 channel analog switch (D1), which under control of the exponent bits, selects the appropriate output of the R/2R ladder. The lowest step of the ladder is connected to 2 inputs of D1 to make the step size for the 2 halves of segment 1 the same. D2 buffers the output of D1.

Some points to note about the decoder are:

(i) Only a 7 bit linear D/A is required for PCM decoding (6 for encoding), making the ratio between the smallest and the largest resistor in the resistor network small, as compared to a 12 bit D/A.

(ii) The same R/2R attenuator is used for both positive and negative analog polarities, making the steps between segments equal for both polarities as required.

3.2.3 Zeltex Linear A/D Module With Digital Companding. This encoder utilises a 10 bit Zeltex linear A/D module, together with a digital compandor, as a PCM encoder. A circuit of the encoder is shown in circuit 7. A 12 bit version of the Zeltex linear A/D module is available using the same pin configuration as the 10 bit, but the conversion time is too slow. The exclusive Or gates connected to the digital outputs of the A/D converter provide PCM code conversion under control of the sign bit. The NH0023 provides the sample and hold facility.

A circuit of the digital compandor is shown in circuit 8. A 9318 priority encoder is used to determine the position of the most significant "1" (excluding the sign bit) in the 12 bit linear code. Only the position of the most significant "1" in the first seven M.S.B's is determined. A 3 bit code is then generated accordingly, and is inverted to become the exponent bits. The 3 bit code is used to address four data selectors simultaneously, with the outputs of the data selectors forming the mantissa bits. The data selectors are arranged so that four adjacent bits of the 12 bit code are selected at any one time, and the selection of the four bits can slide up or down the linear code according to the state of the exponent bits. Note that the last two inputs to the data selectors are connected together to make the step size for the two halves of segment 1 the same.

No results of measurements on this encoder are given in this report, as results are not comparable with the measurement results of the 12 bit D/A codecs.

3.3 Integrating Ramp Codec. This codec will be fully reported on in the as yet unpublished R.L. Report No. 6611 entitled "An Experimental Integrating Ramp Type PCM Codec" by V.S. Sargeant.

## 4. TESTS PERFORMED ON CODECS

The number of tests that could be performed on PCM codecs is large (e.g. see Ref. 1) and performing them all would require a great deal of time. It was therefore decided to limit the number of tests to three, on the assumption that the three selected give an objective representation of the performance of the codecs.

4.1 Linearity of Segments about AC Zero. This test was performed with the aid of a simple up/down counter circuit as shown in circuit 9. The circuitry is used to generate an 11 bit linear up/down binary count. The eight M.S.B's of the up/down counter are fed into a PCM decoder. The analog output of the decoder is then observed on an oscilloscope. Figure 7 shows a photograph of the analog output of a PCM decoder addressed by the up/down counter. Note that the curve approximates a logarithmic law. The individual steps of segment 7 can also be seen. Figure 7 has been expanded about AC zero in figures 8 to 10 to show the linearity of segment 1 for the various codecs.

4.2 Two Tone Intermodulation Products. The test setup for measurement of two tone intermodulation products is shown in figure 14. C.C.I.T.T. recommendations (Ref. 1), state that the two sine-wave signals in the input level range of -4 to -21 dBm0, should not produce any $2f_1 - f_2$ intermodulation products having a level greater than -35 dB relative to the level of one of the two input signals. All codecs tested meet these recommendations. Results of measurements were similar for all codecs and figures 11 to 13 show typical results for input levels of -21dBm0, -10dBm0, and -4dBm0 respectively.

4.3 Quantization Distortion. The test setup for measurement of Quantization Distortion is shown in figure 16. Results of the measurements on the various codecs are shown in figure 15. The shaded in portion shows the limits as recommended by the C.C.I.T.T. Only the A.W.A. codec does not meet the recommendations, probably due to non-linearities about AC zero.

## 5. CONCLUDING REMARKS

The information gained by the work on single channel PCM codecs has been very valuable. Most of the information can be applied to group codecs in 24 and 30 channel PCM systems, and will help in obtaining a greater understanding of these codecs.

At the present time the uses for single channel PCM codecs are limited. Advancing circuitry miniaturisation techniques and the extension of PCM into the telephone network could mean a greater use for single channel PCM codecs.

ACKNOWLEDGEMENT

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1. C.C.I.T.T. Recommendations G.711 and G.712, Green Book, Vol. III-2, 1973, pp.372-385.

2. H. Kaneko, A Unified Formulation of Segment Companding Laws and Synthesis of Codecs and Digital Compandors, The Bell System Technical Journal, September 1970, Volume 49.

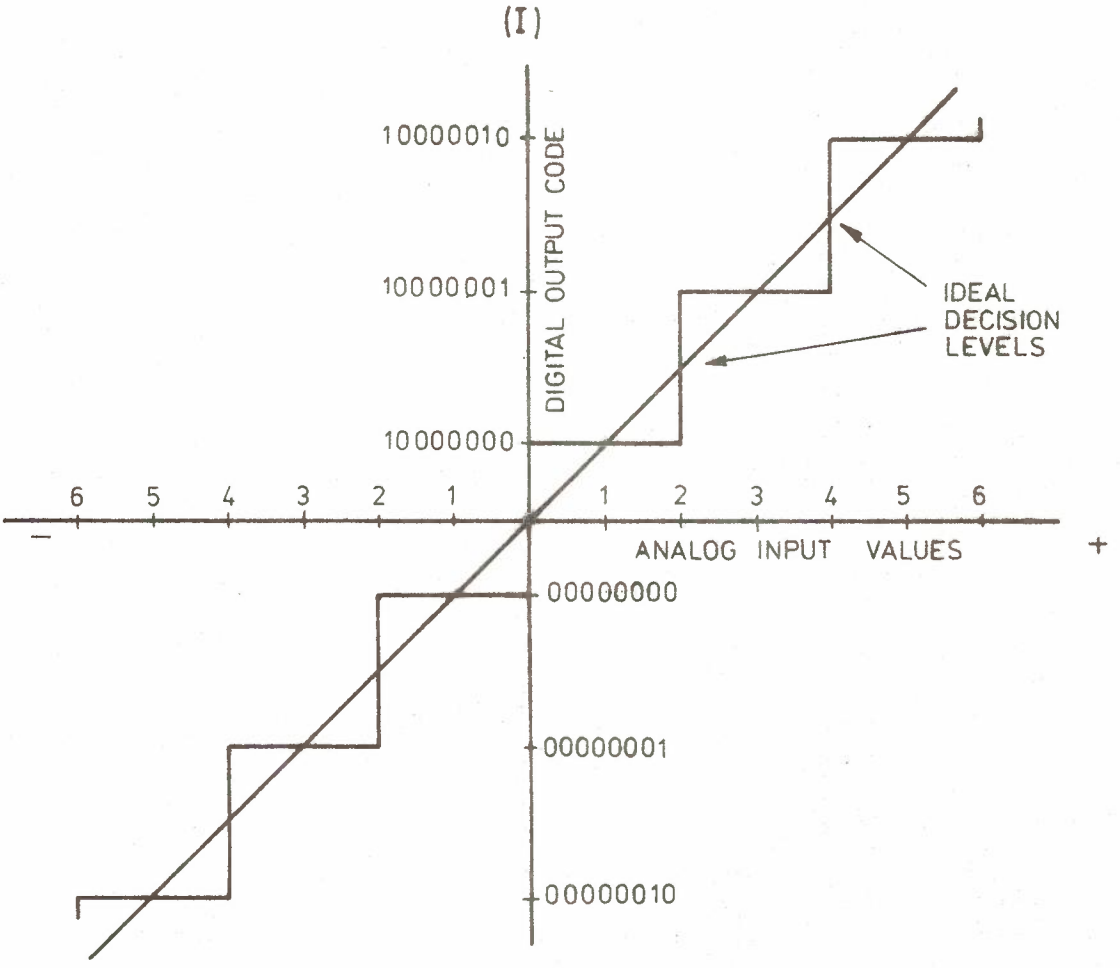



FIG.1. IDEAL A/D CONVERSION ABOUT A.C. ZERO FOR A-LAW ACCORDING TO C.C.I.T.T. RECOMMENDATIONS.

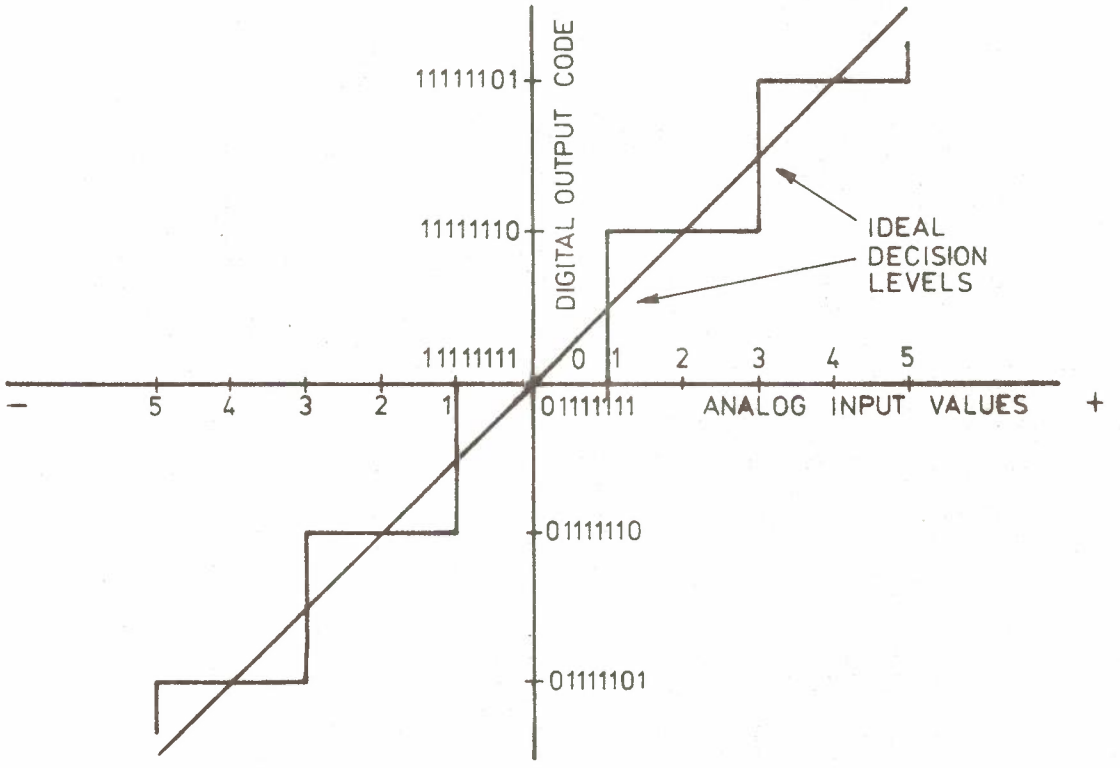



FIG.2. IDEAL A/D CONVERSION ABOUT A.C. ZERO FOR Mu-LAW ACCORDING TO C.C.I.T.T. RECOMMENDATIONS.

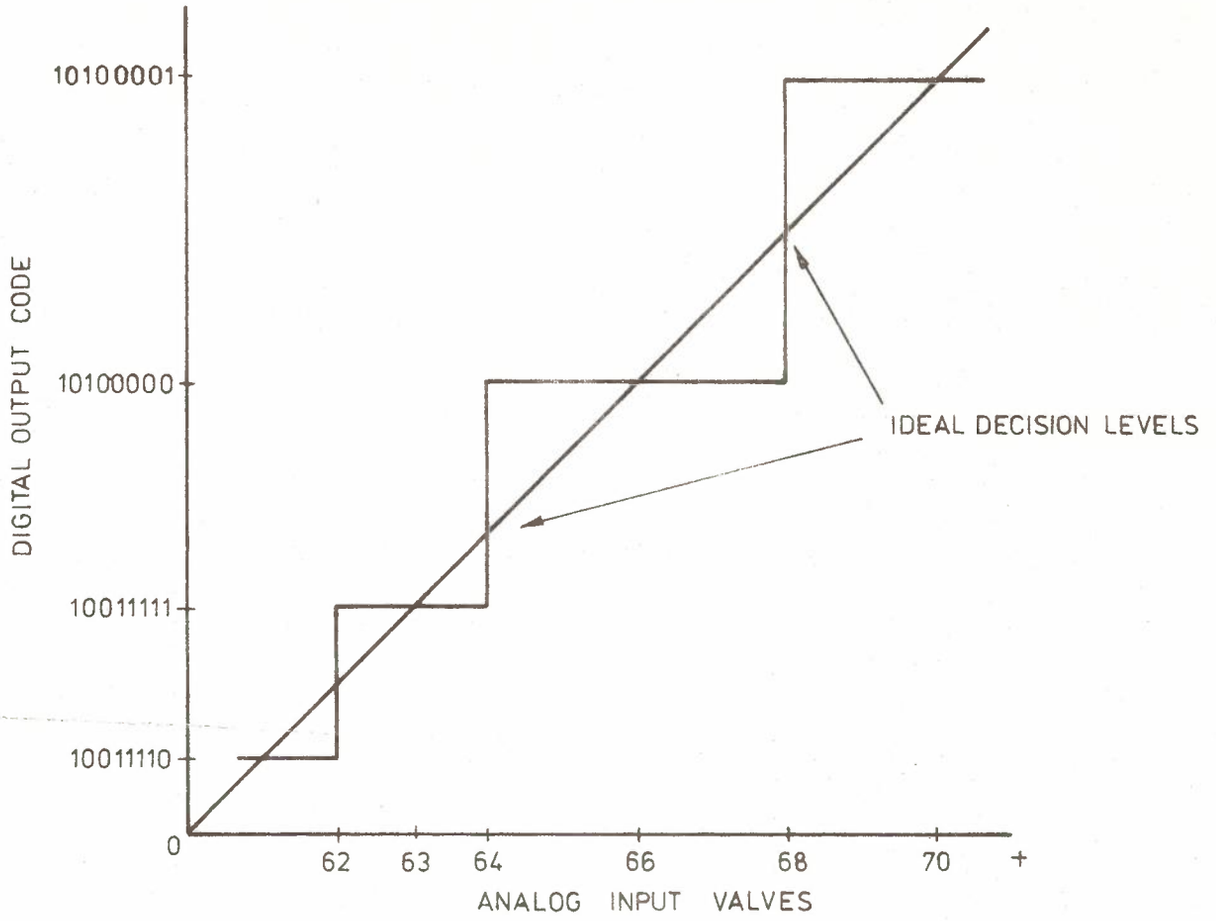



FIG.3. IDEAL A/D CONVERSION BETWEEN SEGMENTS 1 & 2 FOR A-LAW ACCORDING TO C.C.I.T.T. RECOMMENDATIONS.

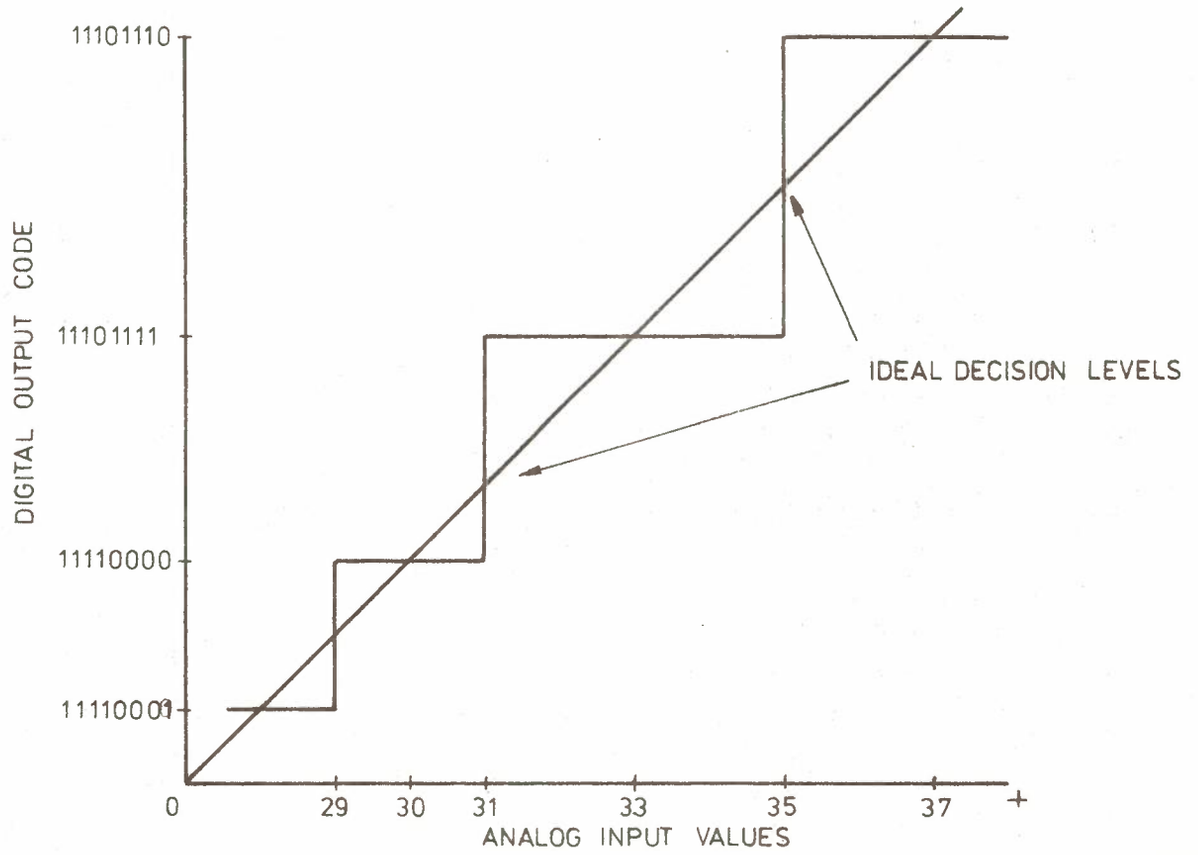



FIG.4. IDEAL A/D CONVERSION BETWEEN SEGMENTS 1 & 2 FOR Mu-LAW ACCORDING TO C.C.I.T.T. RECOMMENDATIONS.

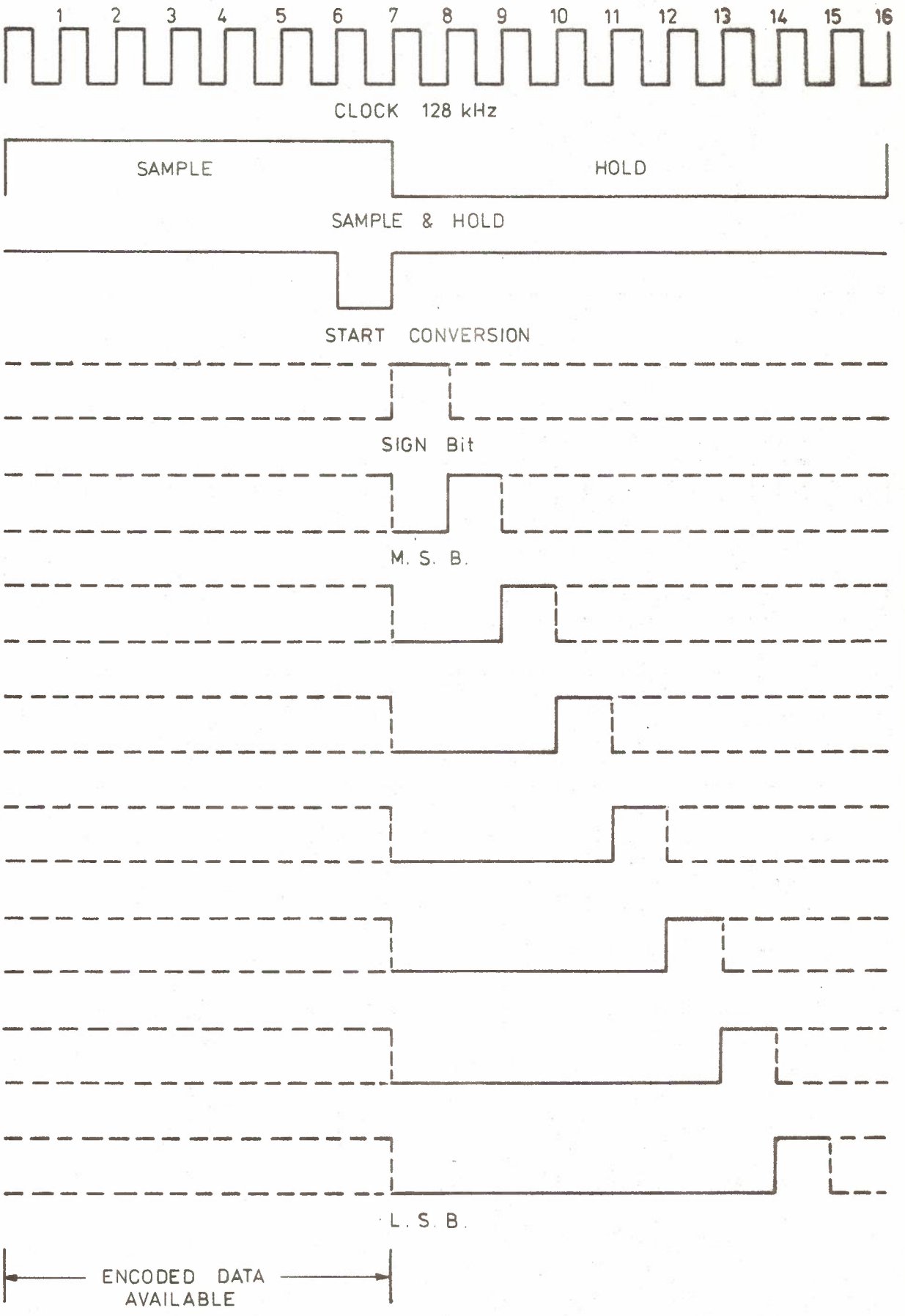



FIG.5 WAVEFORMS FOR ENCODER USING Am 2503.
(DATA Bits INVERTED).

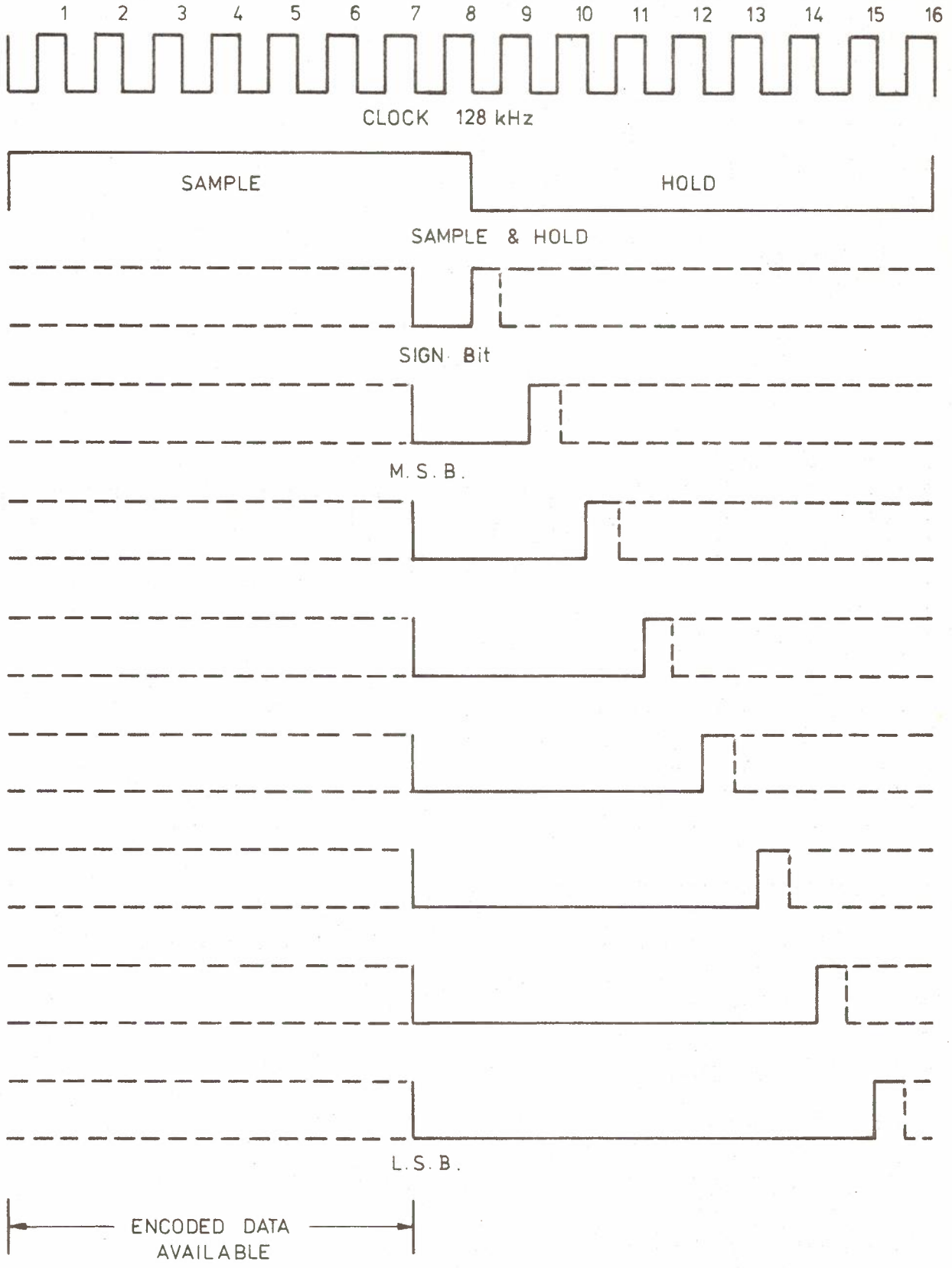



FIG.6. WAVE FORMS FOR ENCODER USING AWM1396.

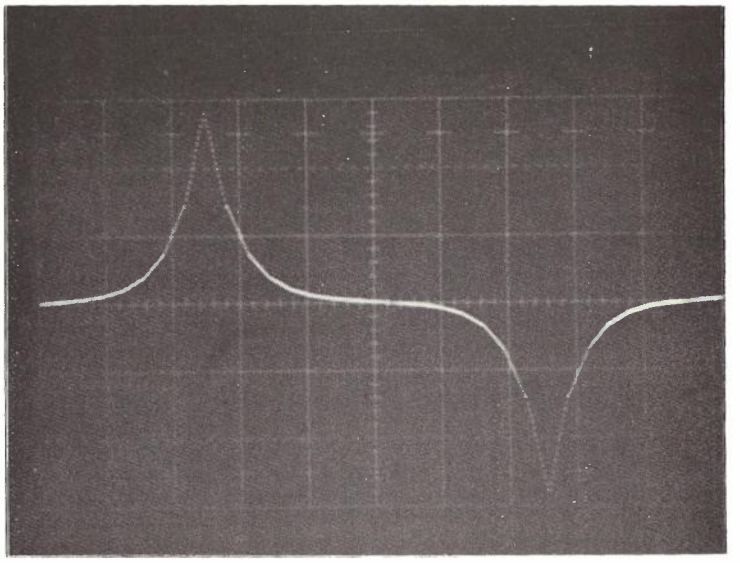


Fig. 7 : Typical analog output of P.C.M. Decoder addressed by binary counter

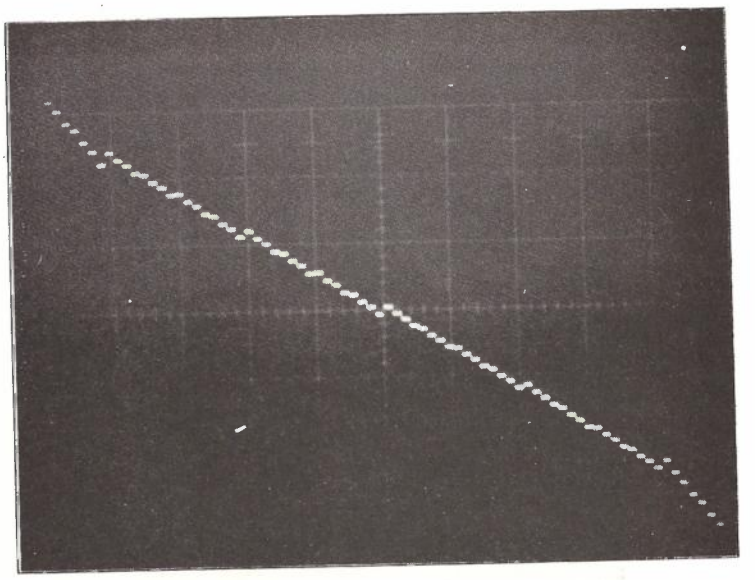


Fig. 8 : Linearity of segments about A.C. zero for A.W.A. decoder

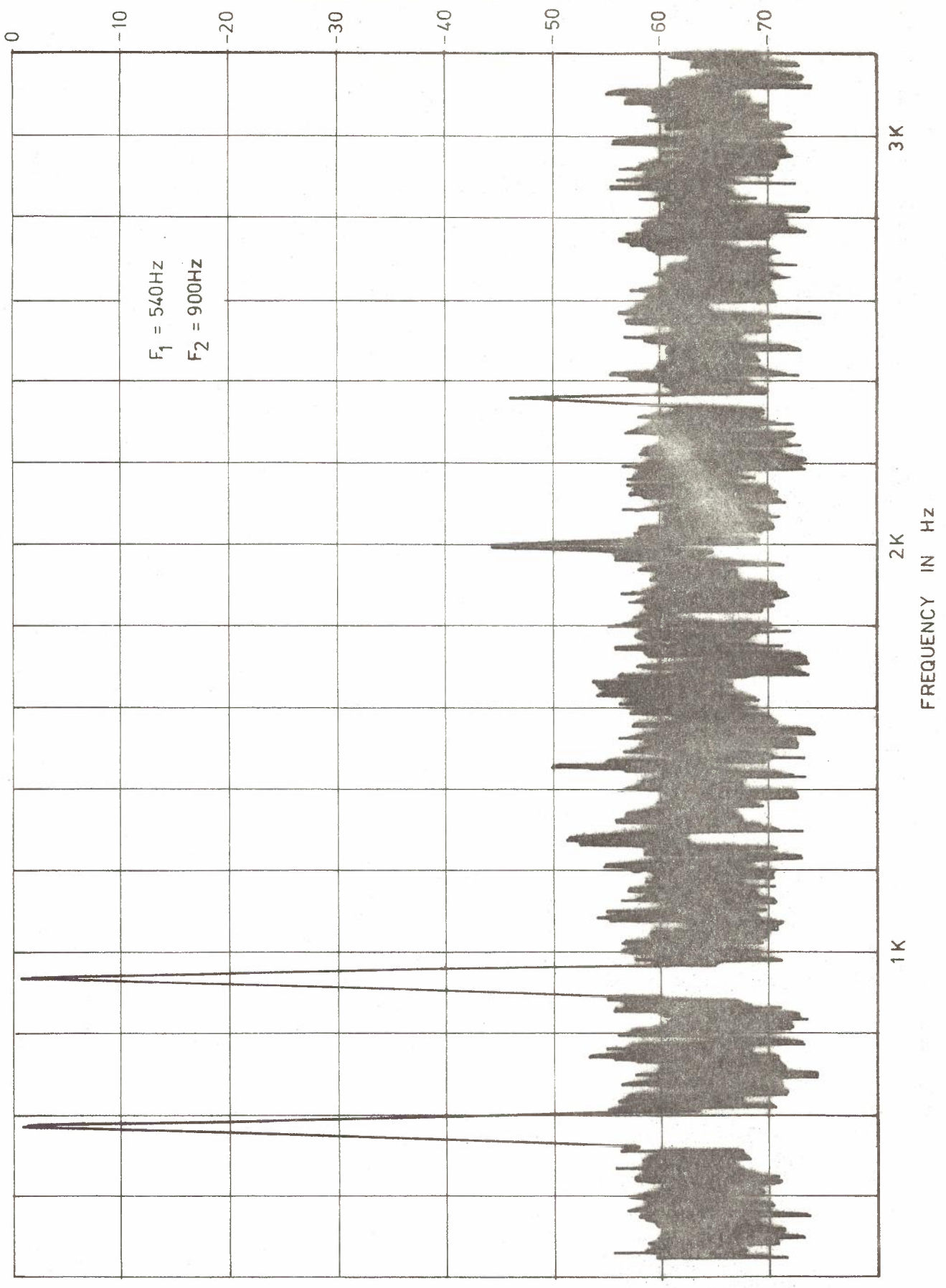



FIG.11. TWO TONE INTERMODULATION PRODUCTS VS FREQUENCY -21dBm0 INPUT LEVEL.

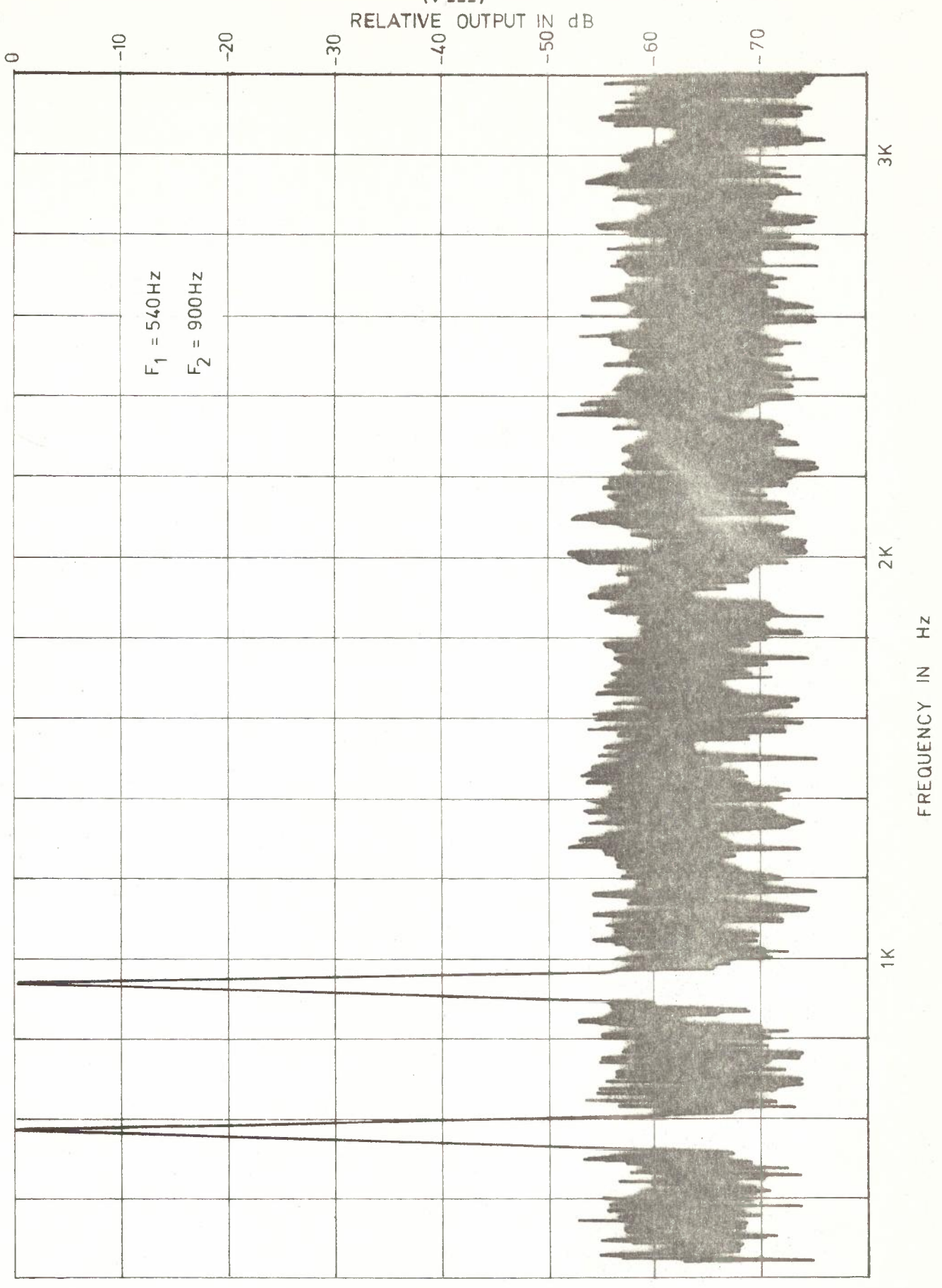



FIG.12. TWO TONE INTERMODULATION PRODUCTS VS FREQUENCY
-10 dBm0 INPUT LEVEL.

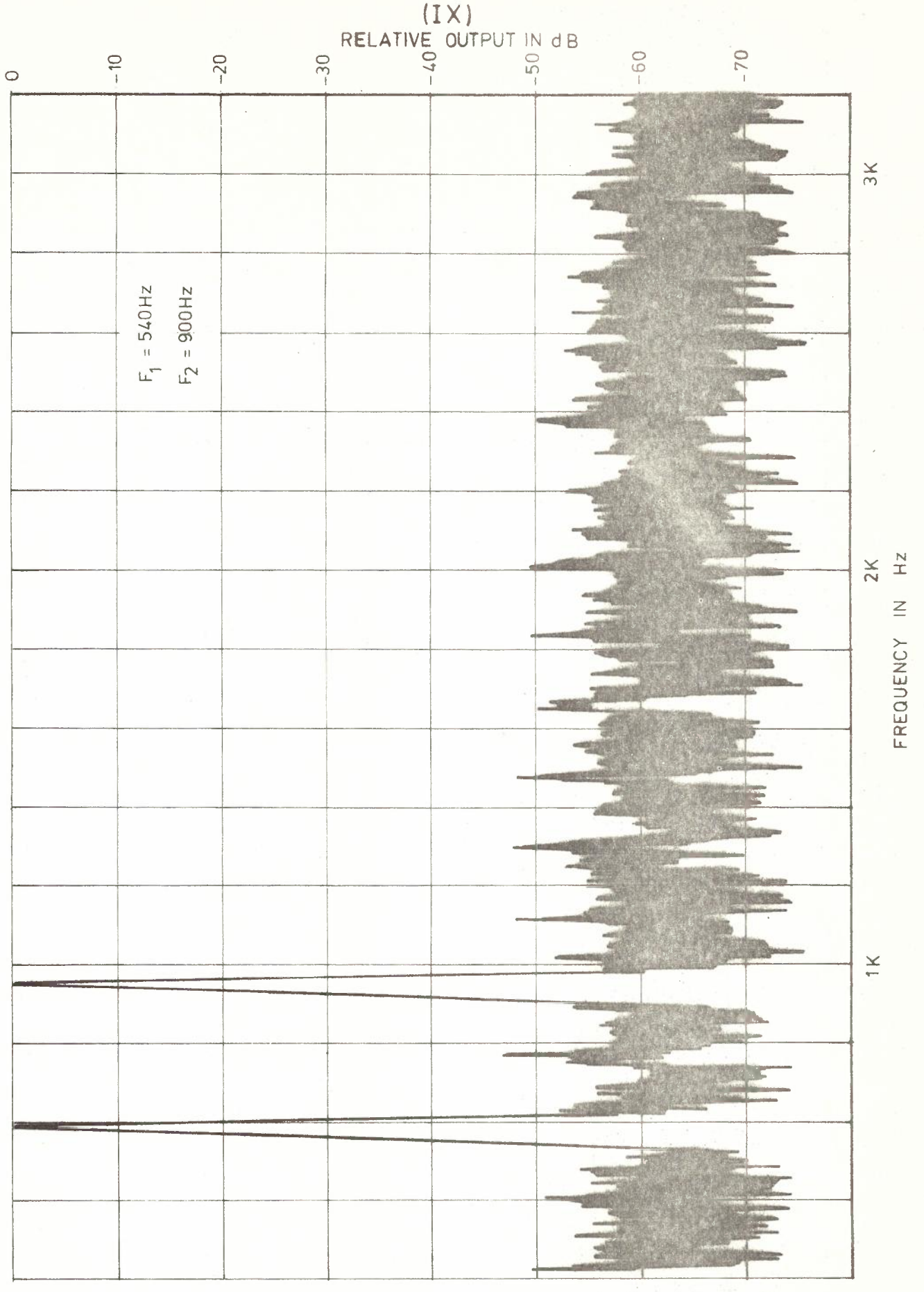



FIG.13. TWO TONE INTERMODULATION PRODUCTS VS FREQUENCY

-4 dBm0 INPUT LEVEL.

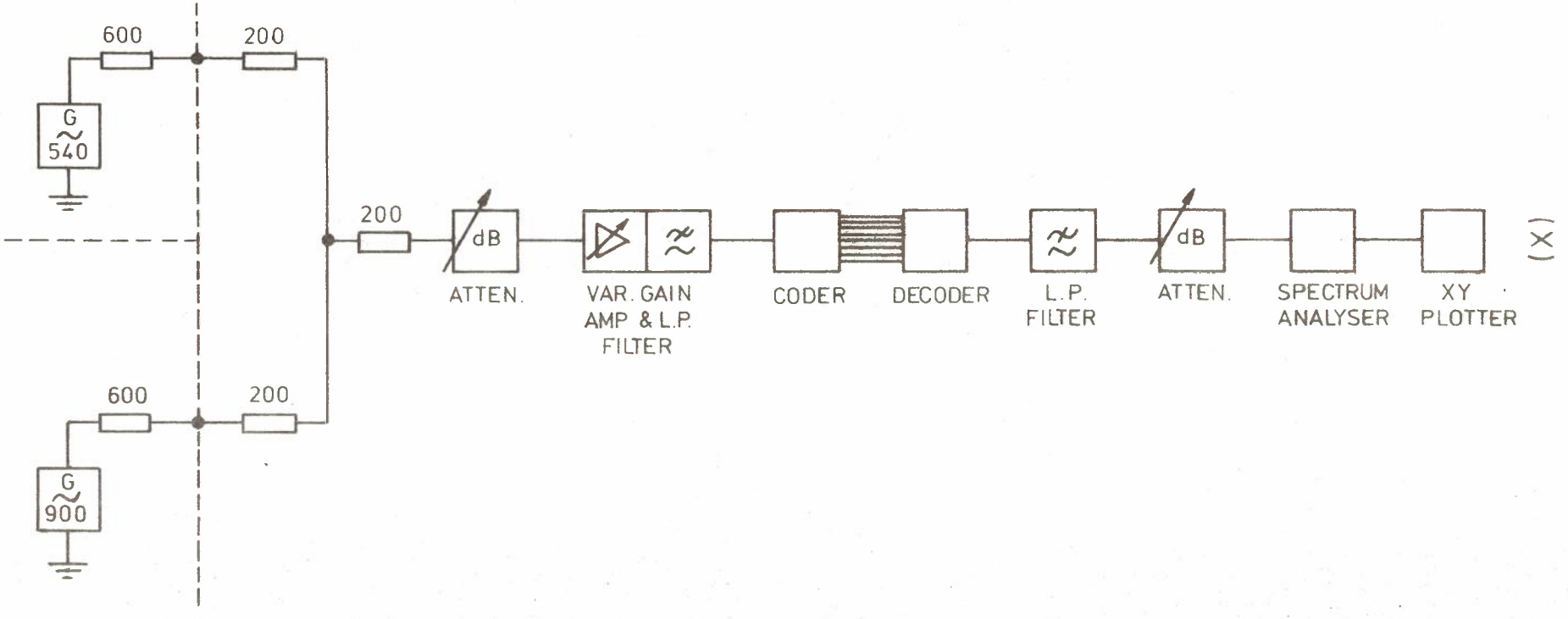



FIG.14. TEST SETUP FOR MEASUREMENT OF TWO TONE INTERMODULATION PRODUCTS.

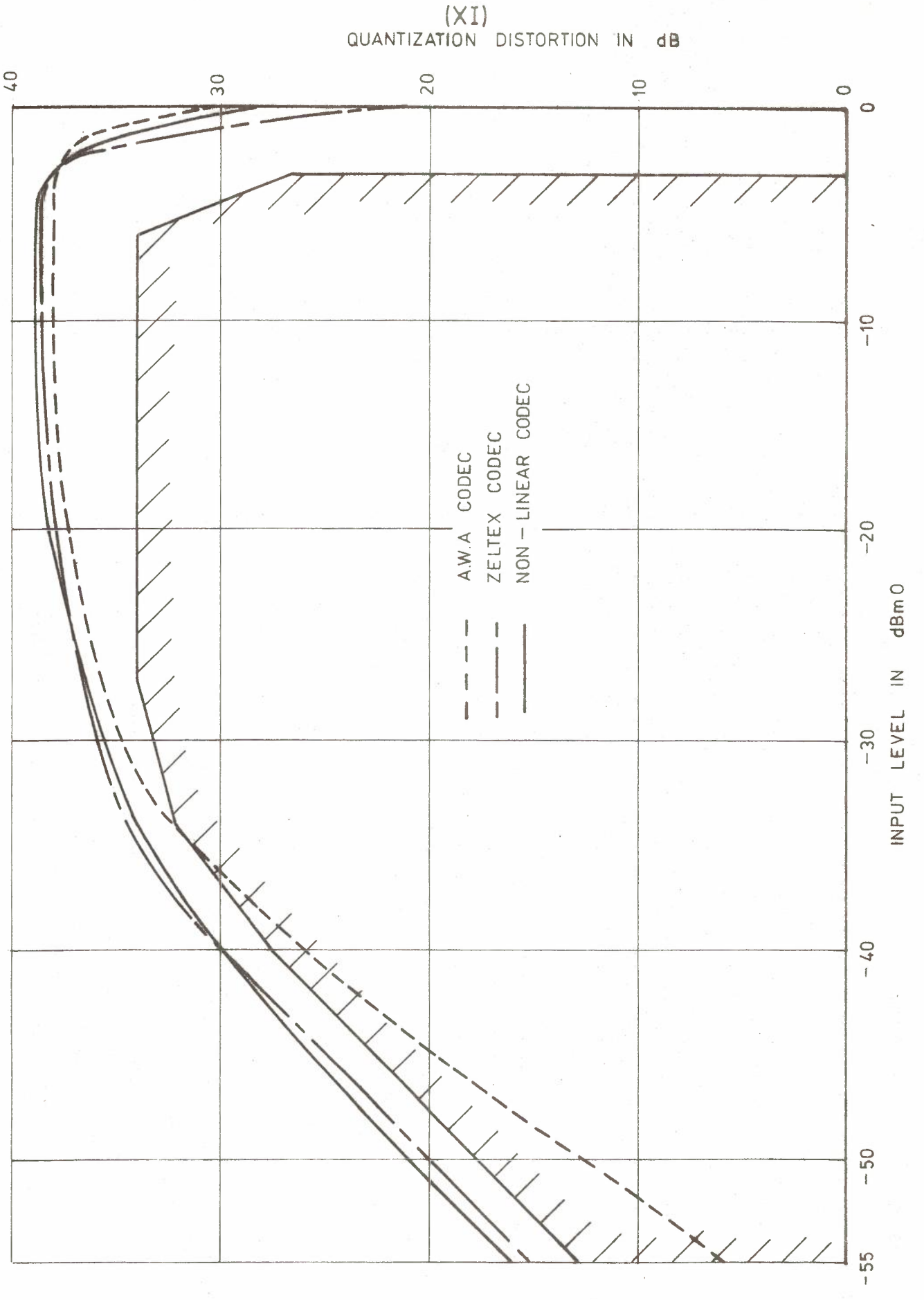



FIG.15. QUANTIZATION DISTORTION VS INPUT LEVEL FOR VARIOUS CODECS.

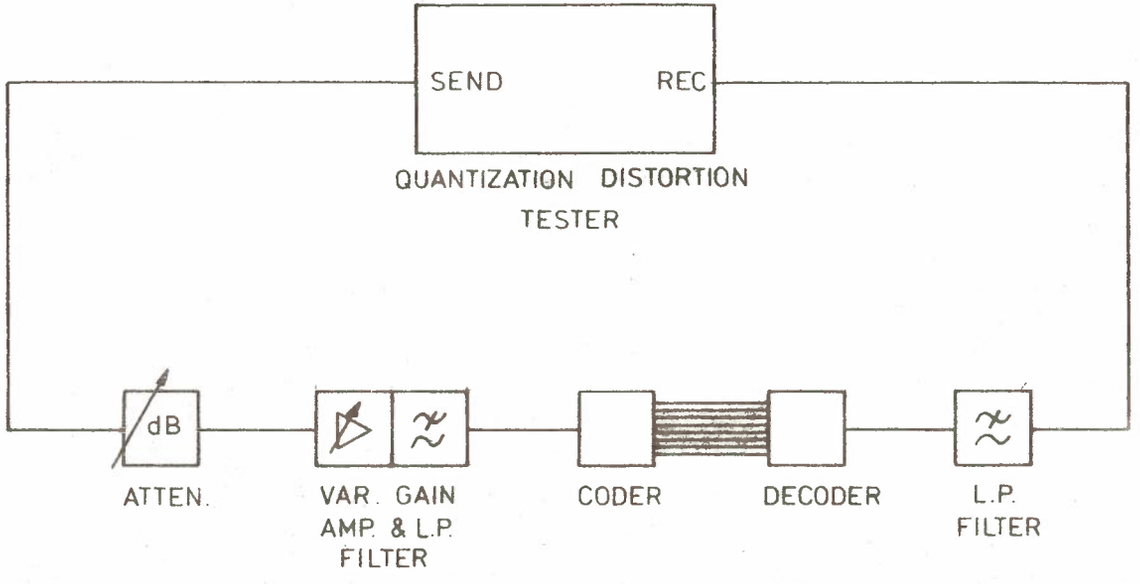



FIG 16. TEST SETUP FOR MEASUREMENT OF QUANTIZATION DISTORTION.

| SEG No. | CODER DECISION AMPLITUDE | BINARY CODE CORRESPONDING TO CODER DECISION AMPLITUDE (12 BITS REQUIRED). | COMPANDED DIGITAL CODE | DECODER OUTPUT AMPLITUDE | BINARY CODE CORRESPONDING TO DECODER OUTPUT AMPLITUDE (13 BITS REQUIRED). |
|---|---|---|---|---|---|
| 7 | 3968 (1984) | S 1 (1 1 1 1) 0 0 0 0 0 0 | S 1 1 1 (1 1 1 1) | 4032 | S 1 (1 1 1 1) 1 0 0 0 0 0 0 |
| | 2176 (1088) | S 1 (0 0 0 1) 0 0 0 0 0 0 | S 1 1 1 (0 0 0 1) | 2112 | S 1 (0 0 0 0) 1 0 0 0 0 0 0 |
| | 2048 (1024) | S 1 (0 0 0 0) 0 0 0 0 0 0 | S 1 1 1 (0 0 0 0) | | |
| 6 | 1984 ( 992) | S 0 1 (1 1 1 1) 0 0 0 0 0 | S 1 1 0 (1 1 1 1) | 2016 | S 0 1 (1 1 1 1) 1 0 0 0 0 0 |
| | 1088 ( 544) | S 0 1 (0 0 0 1) 0 0 0 0 0 | S 1 1 0 (0 0 0 1) | 1056 | S 0 1 (0 0 0 0) 1 0 0 0 0 0 |
| | 1024 ( 512) | S 0 1 (0 0 0 0) 0 0 0 0 0 | S 1 1 0 (0 0 0 0) | 1008 | S 0 0 1 (1 1 1 1) 1 0 0 0 0 |
| 5 | 992 ( 496) | S 0 0 1 (1 1 1 1) 0 0 0 0 | S 1 0 1 (1 1 1 1) | | |
| | 544 ( 272) | S 0 0 1 (0 0 0 1) 0 0 0 0 | S 1 0 1 (0 0 0 1) | 528 | S 0 0 1 (0 0 0 0) 1 0 0 0 0 |
| | 512 ( 256) | S 0 0 1 (0 0 0 0) 0 0 0 0 | S 1 0 1 (0 0 0 0) | 504 | S 0 0 0 1 (1 1 1 1) 1 0 0 0 |
| 4 | 496 ( 248) | S 0 0 0 1 (1 1 1 1) 0 0 0 | S 1 0 0 (1 1 1 1) | | |
| | 272 ( 136) | S 0 0 0 1 (0 0 0 1) 0 0 0 | S 1 0 0 (0 0 0 1) | 264 | S 0 0 0 1 (0 0 0 0) 1 0 0 0 |
| | 256 ( 128) | S 0 0 0 1 (0 0 0 0) 0 0 0 | S 1 0 0 (0 0 0 0) | 252 | S 0 0 0 0 1 (1 1 1 1) 1 0 0 |
| 3 | 248 ( 124) | S 0 0 0 0 1 (1 1 1 1) 0 0 | S 0 1 1 (1 1 1 1) | | |
| | 136 ( 68) | S 0 0 0 0 1 (0 0 0 1) 0 0 | S 0 1 1 (0 0 0 1) | 132 | S 0 0 0 0 1 (0 0 0 0) 1 0 0 |
| | 128 ( 64) | S 0 0 0 0 1 (0 0 0 0) 0 0 | S 0 1 1 (0 0 0 0) | 126 | S 0 0 0 0 0 1 (1 1 1 1) 1 0 |
| 2 | 124 ( 62) | S 0 0 0 0 0 1 (1 1 1 1) 0 | S 0 1 0 (1 1 1 1) | | |
| | 68 ( 34) | S 0 0 0 0 0 1 (0 0 0 1) 0 | S 0 1 0 (0 0 0 1) | 66 | S 0 0 0 0 0 1 (0 0 0 0) 1 0 |
| | 64 ( 32) | S 0 0 0 0 0 1 (0 0 0 0) 0 | S 0 1 0 (0 0 0 0) | 63 | S 0 0 0 0 0 0 1 (1 1 1 1) 1 |
| 1 | 62 ( 31) | S 0 0 0 0 0 0 1 (1 1 1 1) | S 0 0 1 (1 1 1 1) | | |
| | 34 ( 17) | S 0 0 0 0 0 0 1 (0 0 0 1) | S 0 0 1 (0 0 0 1) | 33 | S 0 0 0 0 0 0 1 (0 0 0 0) 1 |
| | 32 ( 16) | S 0 0 0 0 0 0 1 (0 0 0 0) | S 0 0 1 (0 0 0 0) | 31 | S 0 0 0 0 0 0 0 (1 1 1 1) 1 |
| | 30 ( 15) | S 0 0 0 0 0 0 0 (1 1 1 1) | S 0 0 0 (1 1 1 1) | | |
| | 2 ( 1) | S 0 0 0 0 0 0 0 (0 0 0 1) | S 0 0 0 (0 0 0 1) | 1 | S 0 0 0 0 0 0 0 (0 0 0 0) 1 |
| | 0 | S 0 0 0 0 0 0 0 (0 0 0 0) | S 0 0 0 (0 0 0 0) | | |

S = SIGN BIT.

TABLE 1. A - LAW CODING / DECODING

| SEGMENT | COMPRESSED CODE | LINEAR REPRESENTATION |
|---|---|---|
| 8 (7) | S 1 1 1 W X Y Z | S 1 W X Y Z 0 0 0 0 0 0 |
| 7 (6) | S 1 1 0 W X Y Z | S 0 1 W X Y Z 0 0 0 0 0 |
| 6 (5) | S 1 0 1 W X Y Z | S 0 0 1 W X Y Z 0 0 0 0 |
| 5 (4) | S 1 0 0 W X Y Z | S 0 0 0 1 W X Y Z 0 0 0 |
| 4 (3) | S 0 1 1 W X Y Z | S 0 0 0 0 1 W X Y Z 0 0 |
| 3 (2) | S 0 1 0 W X Y Z | S 0 0 0 0 0 1 W X Y Z 0 |
| 2 (1) | S 0 0 1 W X Y Z | S 0 0 0 0 0 0 1 W X Y Z |
| 1 (1) | S 0 0 0 W X Y Z | S 0 0 0 0 0 0 0 W X Y Z |

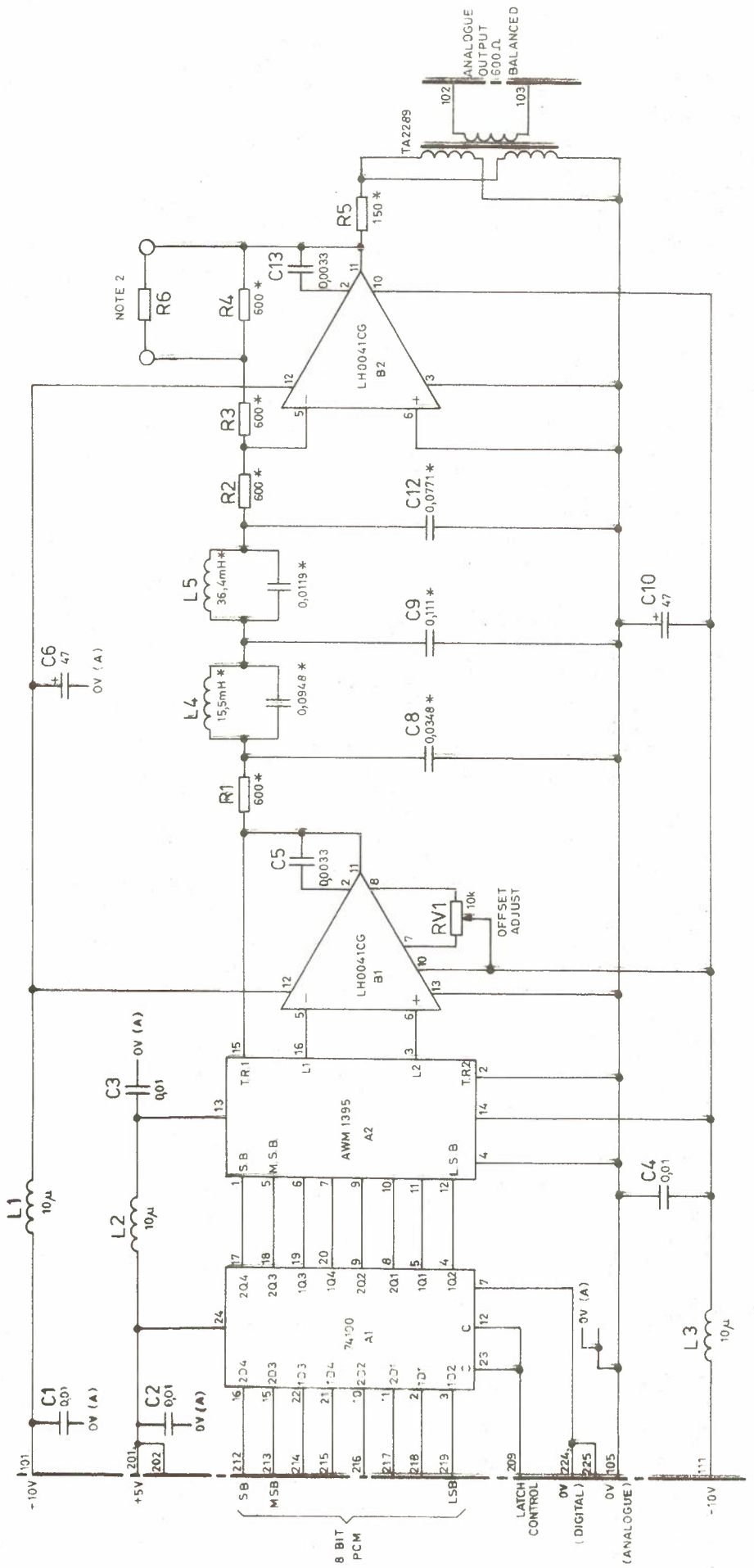
S = SIGN BIT.

TABLE 2. COMPANDED DIGITAL CODE AND LINEAR REPRESENTATION OF A - LAW

| SEG. No. | CODER DECISION AMPLITUDE | BINARY CODE CORRESPONDING TO CODER DECISION AMPLITUDE (14 BITS REQUIRED). | COMPANDED DIGITAL CODE | DECODER OUTPUT AMPLITUDE | BINARY CODE CORRESPONDING TO DECODER OUTPUT AMPLITUDE (13 BITS REQUIRED). |
|---|---|---|---|---|---|
| 8 | 7903 | S11111011111111 | S00000000 | 8031 | S1111101111111 |
| | 4319 | S10000101111111 | S00001110 | 4191 | S1000001011111 |
| | 4063 | S01111101111111 | S00001111 | 3999 | S0111110011111 |
| 7 | 3935 | S01111001111111 | S00010000 | 2079 | S0100000011111 |
| | 2143 | S01000010111111 | S00011110 | 1983 | S0011110111111 |
| | 2015 | S00111110111111 | S00011111 | 1023 | S0000111111111 |
| 6 | 1951 | S00111100111111 | S01000000 | 975 | S0000111001111 |
| | 1055 | S00100000111111 | S01011110 | 495 | S0000111101111 |
| | 991 | S00011110111111 | S01011111 | 471 | S0000111010111 |
| 5 | 959 | S00011101111111 | S01100000 | 231 | S0000011100111 |
| | 511 | S00001111111111 | S01111110 | 219 | S0000011011011 |
| | 479 | S00001110111111 | S01111111 | 99 | S0000001100011 |
| 4 | 463 | S00001110011111 | S10000000 | 93 | S0000001011101 |
| | 239 | S00000111011111 | S10011110 | 33 | S0000000100001 |
| | 223 | S00000110111111 | S10011111 | 30 | S0000000011110 |
| 3 | 215 | S00000110101111 | S10100000 | 2 | S0000000000010 |
| | 103 | S00000011101111 | S10111110 | 0 | S0000000000000 |
| | 95 | S00000010111111 | S10111111 | | |
| 2 | 91 | S00000010110111 | S11000000 | | |
| | 35 | S00000001000111 | S11011110 | | |
| | 31 | S00000000111111 | S11011111 | | |
| 1 | 29 | S00000000111101 | S11100000 | | |
| | 3 | S00000000000011 | S11111101 | | |
| | 1 | S00000000000001 | S11111110 | | |
| | 0 | S00000000000000 | S11111111 | | |

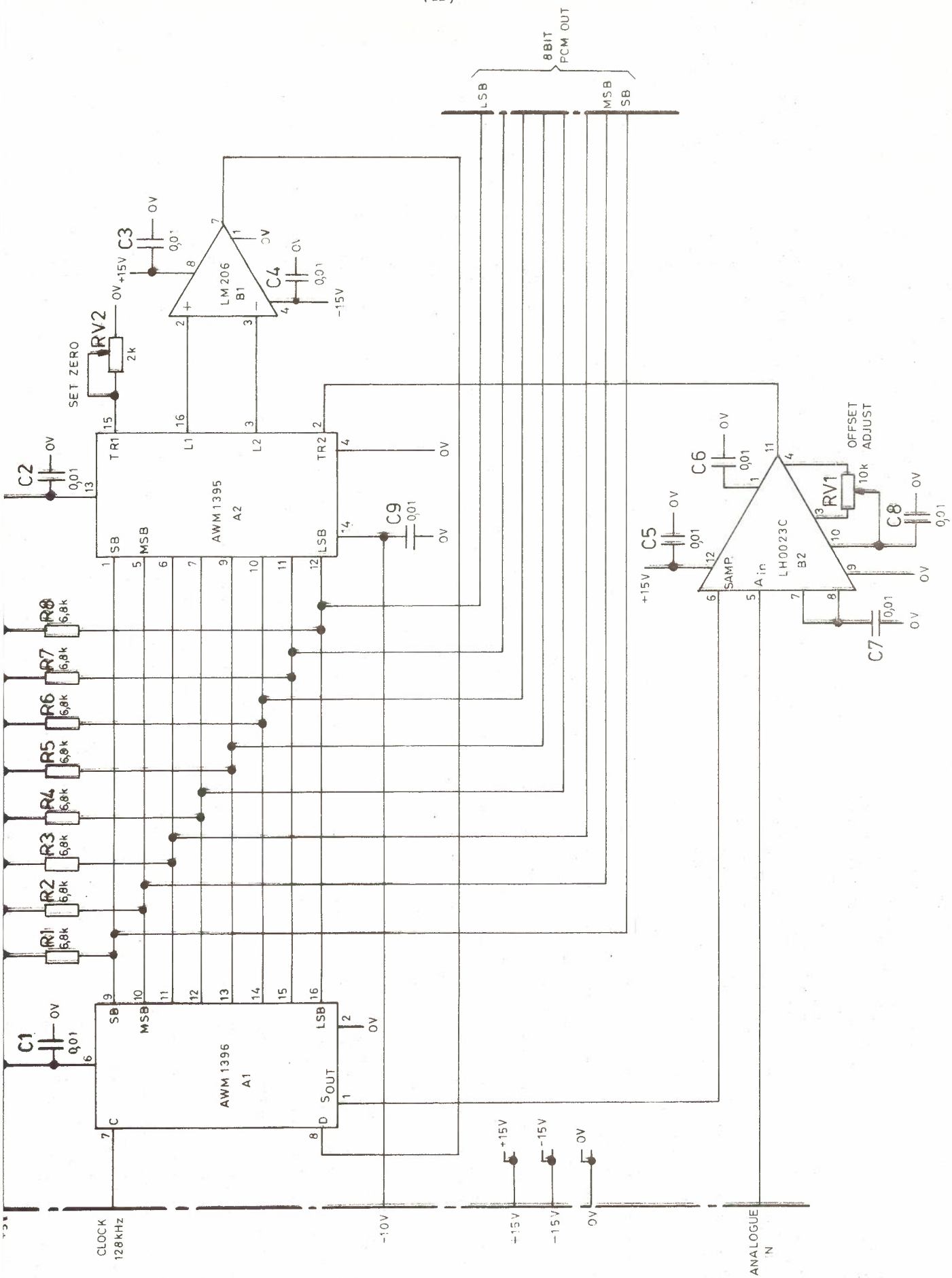
S= SIGN BIT.

TABLE 3. Mu - LAW CODING / DECODING.

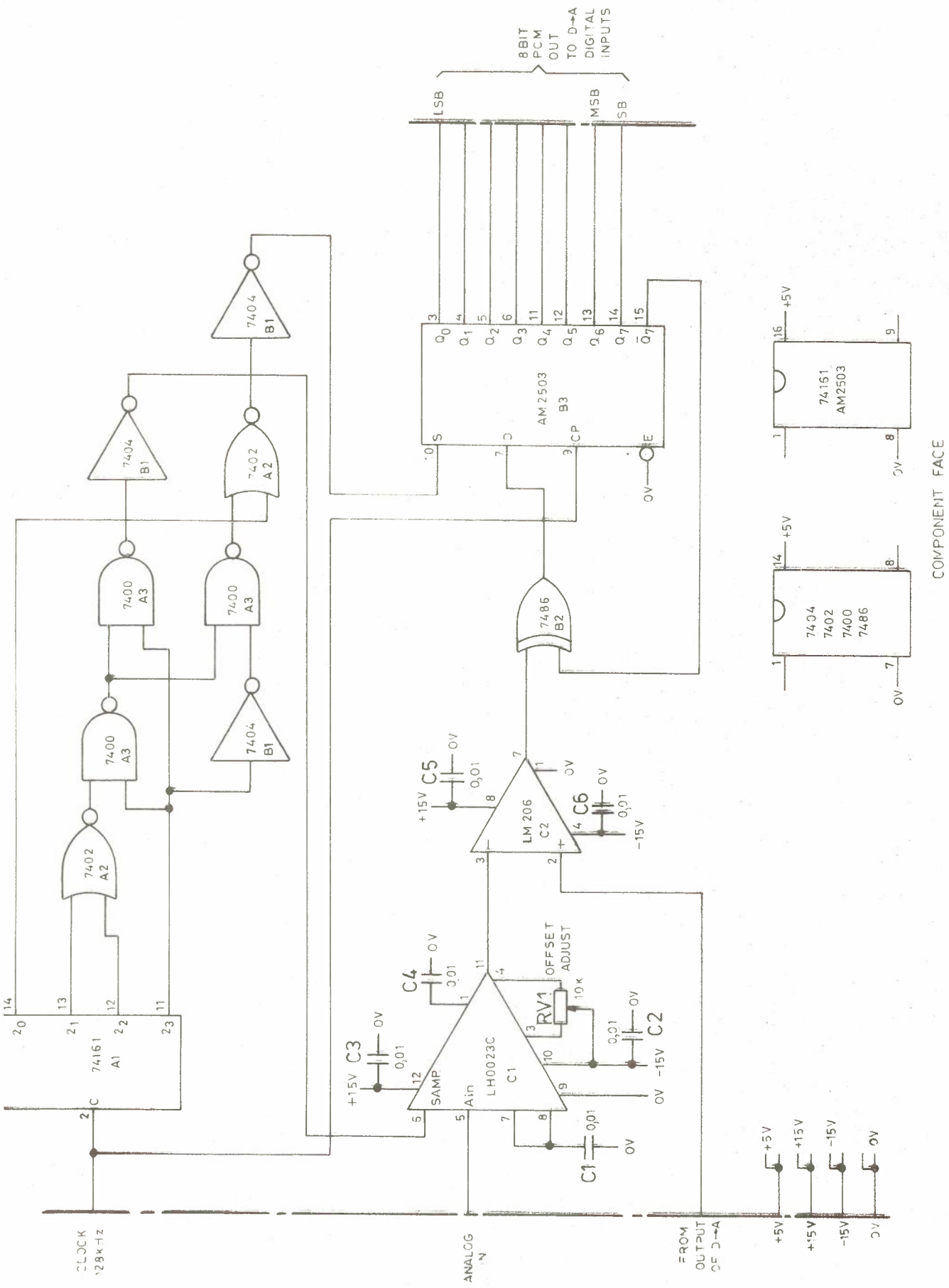



NOTES:
1 MOUNTED ON RPC 1768A
2 SELECT VALUE TO SET OUTPUT LEVEL
3 COMPONENTS MARKED * ± 1%.

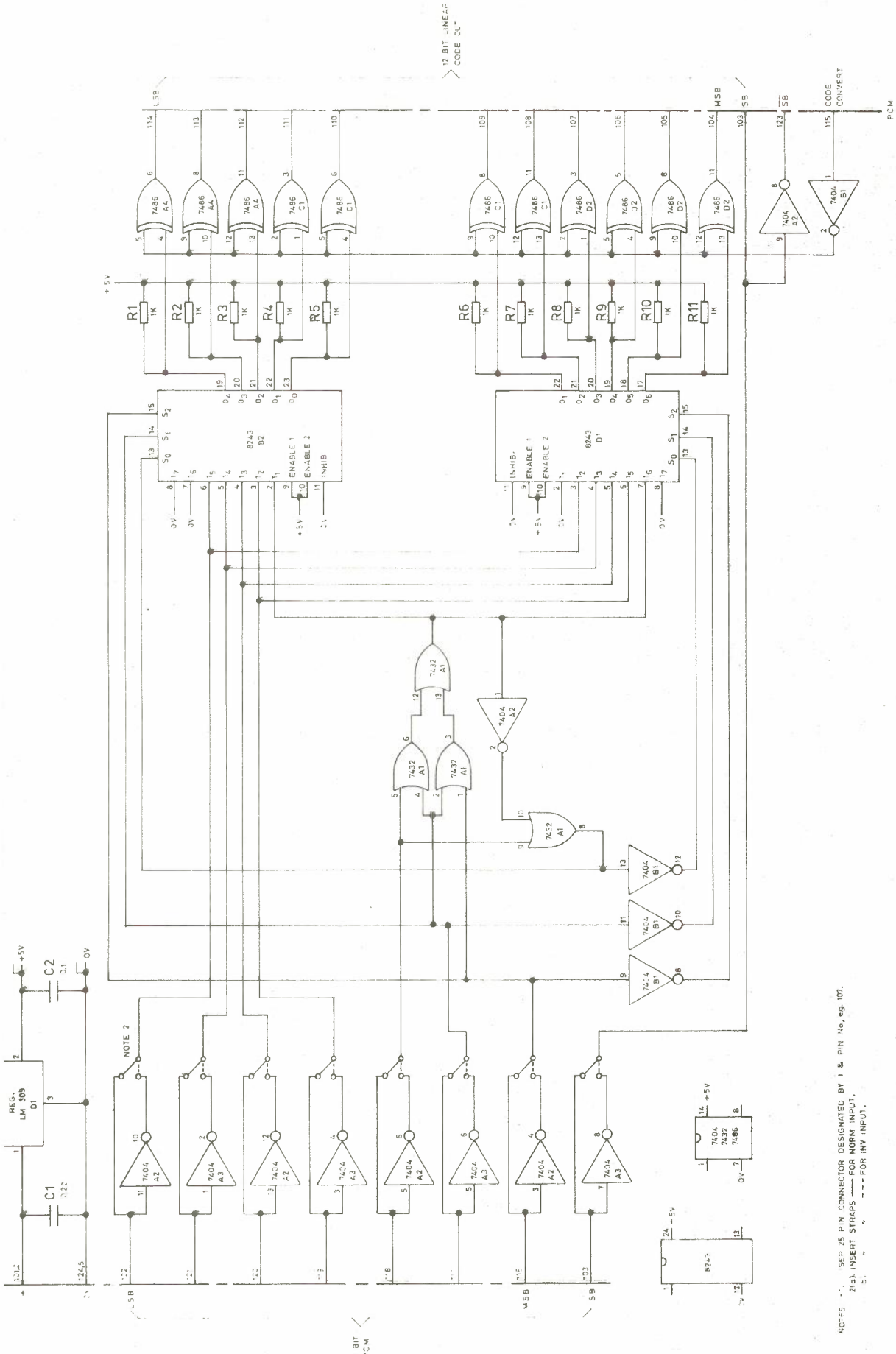
CIRCUIT 1. P.C.M. DECODER USING AWM 1395
CIRCUIT DIAGRAM.



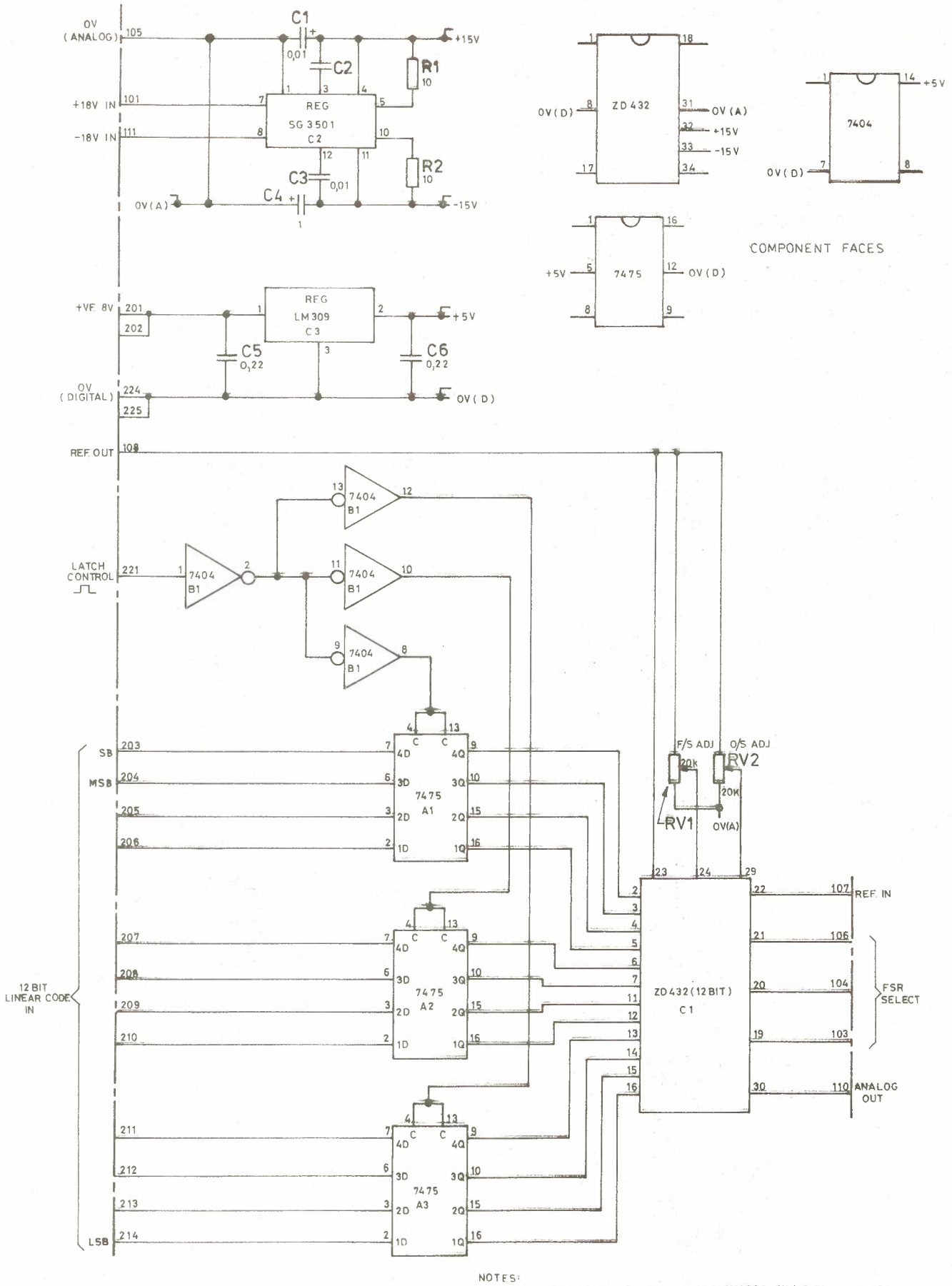

CIRCUIT 2. PCM ENCODER USING AWM 1395/1396
CIRCUIT DIAGRAM.




CIRCUIT 3 SUCCESSIVE APPROXIMATION CONTROL LOGIC
CIRCUIT DIAGRAM.

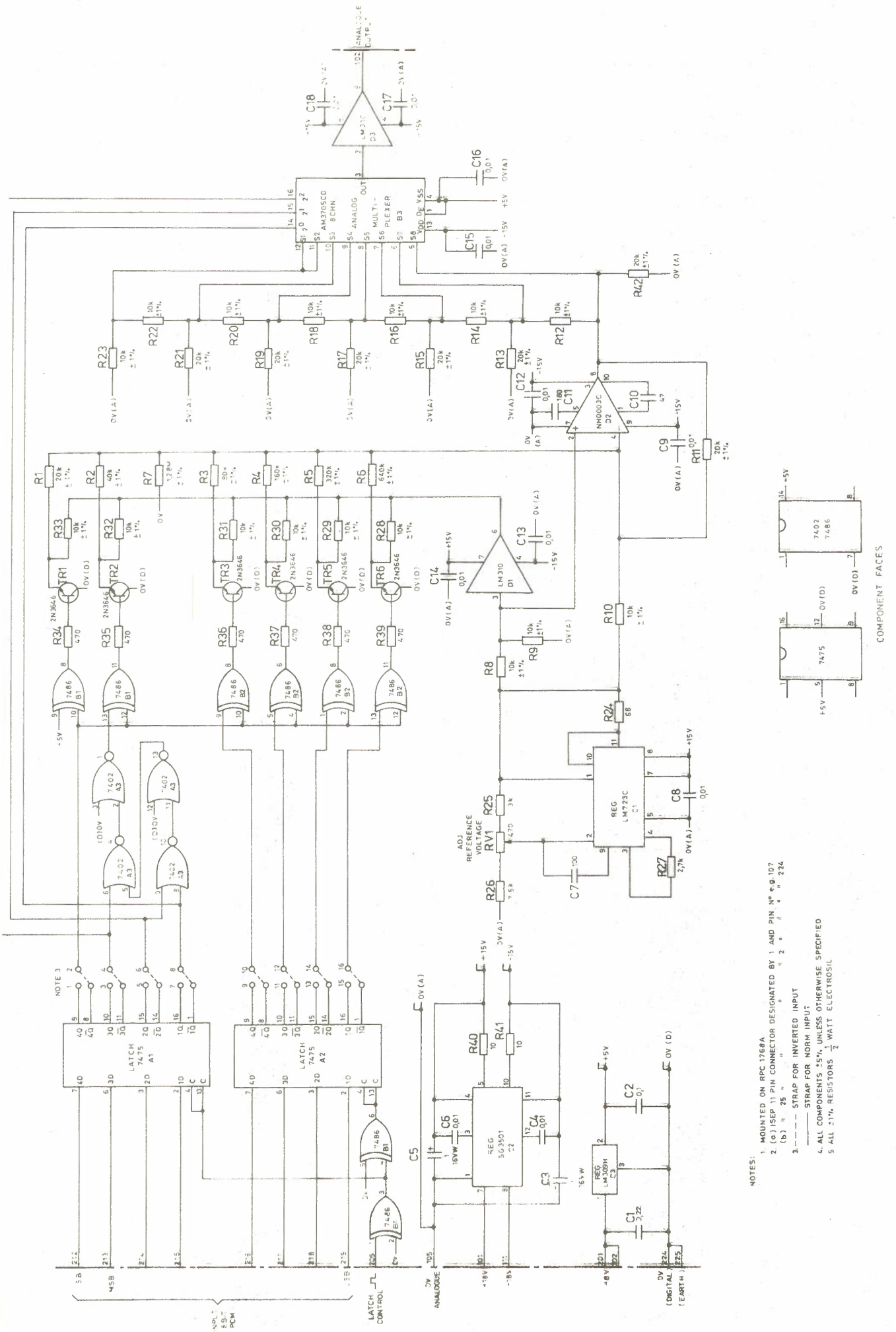



CIRCUIT 4. 8 BIT P.C.M. TO 12 BIT LINEAR CODE CONVERTOR
CIRCUIT DIAGRAM.

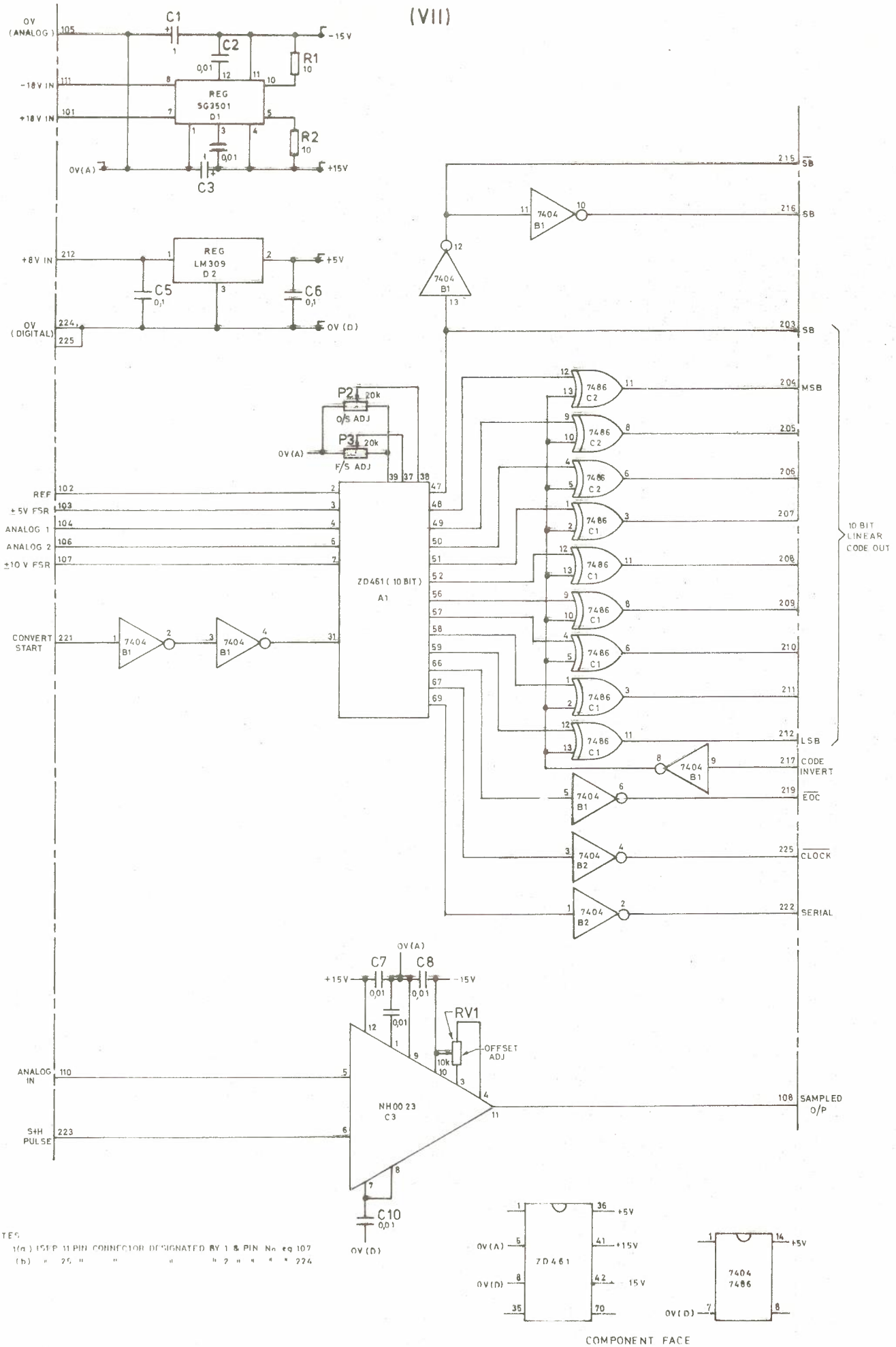



NOTES:
1(a) ISEP 11 PIN CONNECTOR DESIGNATED BY 1 & PIN No eg 107
(b) " 25 " " " " " 2 " " " " 224

CIRCUIT 5. 12 BIT LINEAR D/A CONVERTOR
CIRCUIT DIAGRAM.



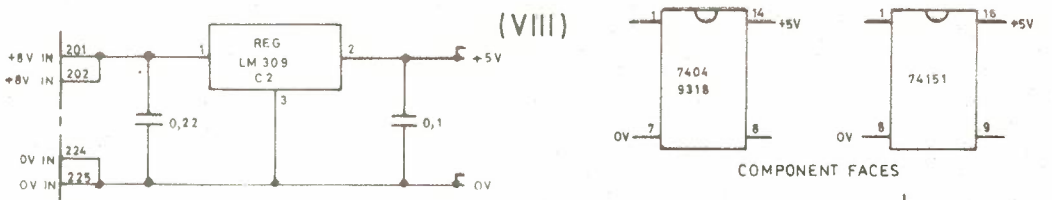

CIRCUIT 6. NON LINEAR DECODER
CIRCUIT DIAGRAM.

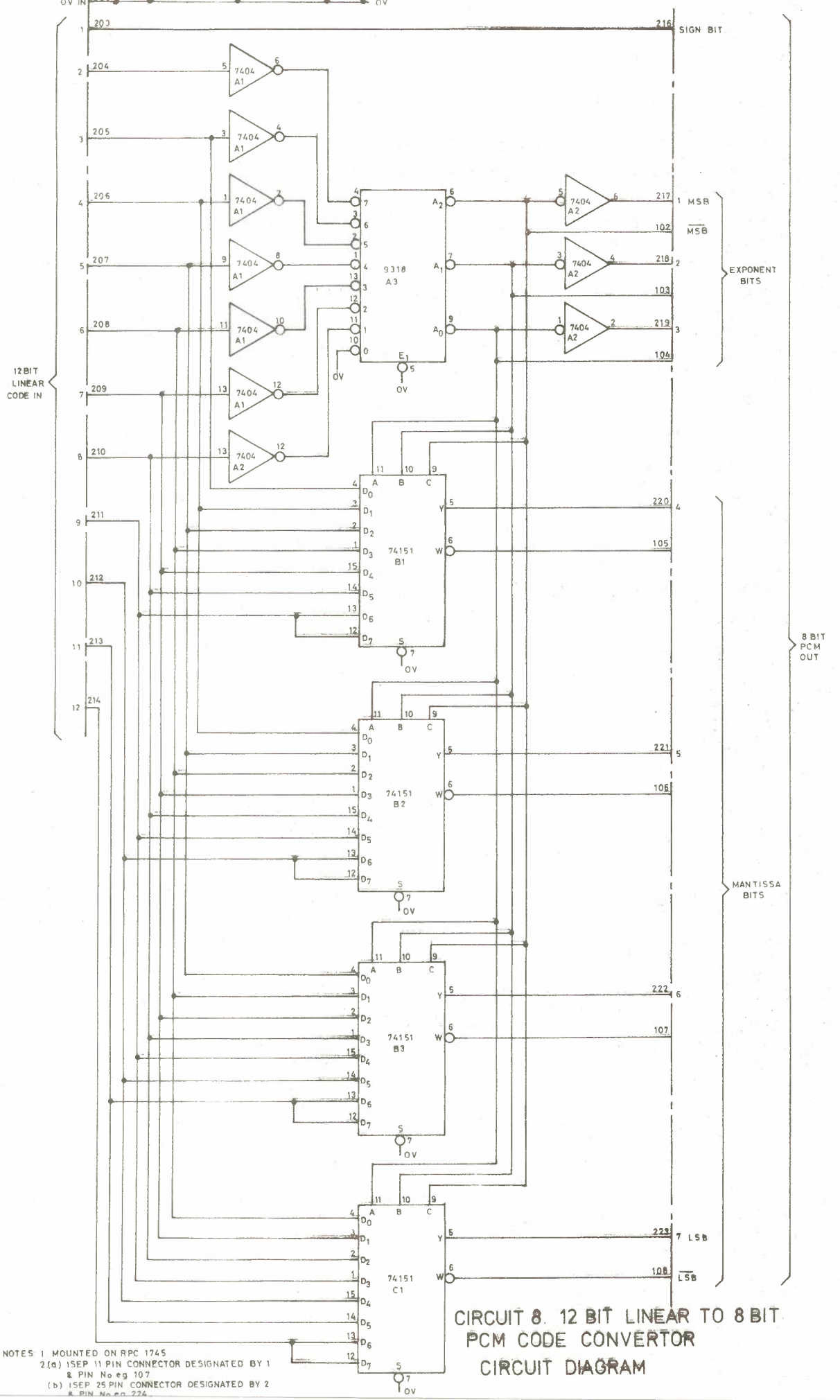



NOTES

1(a) ISEP 11 PIN CONNECTOR DESIGNATED BY 1 & PIN No. eg 107
(b) " 25 " " " " " 2 " " " " 224

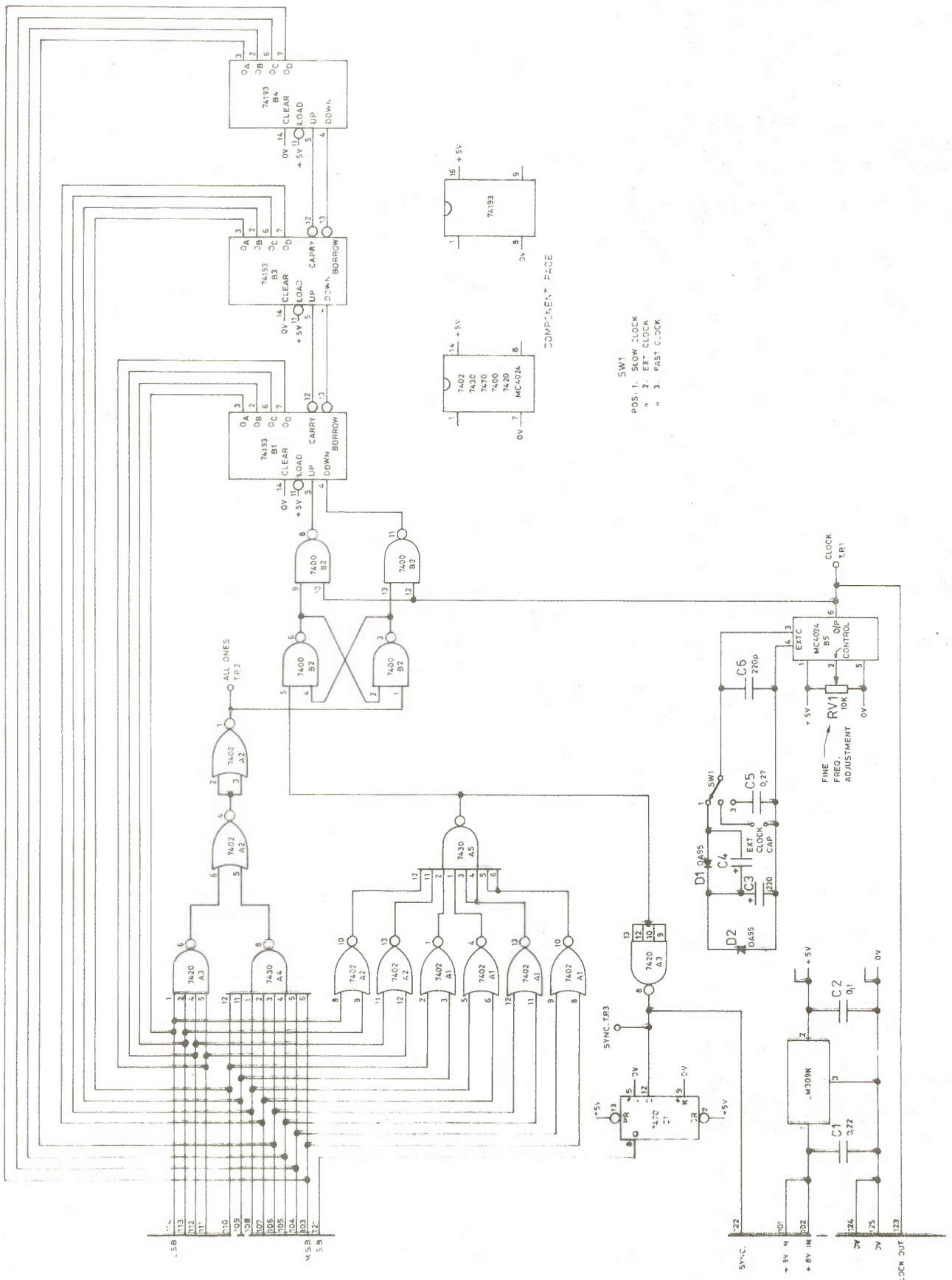
CIRCUIT 7. 10 BIT LINEAR A/D CONVERTOR
CIRCUIT DIAGRAM.




NOTES 1 MOUNTED ON RPC 1745
2(a) ISEP 11 PIN CONNECTOR DESIGNATED BY 1
& PIN No eg 107
(b) ISEP 25 PIN CONNECTOR DESIGNATED BY 2
& PIN No eg 224

CIRCUIT 8. 12 BIT LINEAR TO 8 BIT PCM CODE CONVERTOR CIRCUIT DIAGRAM




CIRCUIT 9. D/A CONVERTOR TESTER
CIRCUIT DIAGRAM.