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REPORT 7057

LABORATORY TESTS ON A NEC 6312 KBIT/S AND A GEC 8448 KBIT/S SECOND ORDER DIGITAL MULTIPLEX

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BY R.B. COXHILL

As part of the Research Laboratories programme on digital transmission systems, time division multiplexes are being studied with a view to their introduction into the Australian Telecommunications Network.

The C.C.I.T.T. recommendation for first and second level multiplexes are now basically established. On a first network level either 24 or 30 PCM speech channels are multiplexed giving bit rates of 1544 kbit/s and 2048 kbit/s respectively. On a second network level up to four first level PCM systems are multiplexed into a bit stream of either 6312 kbit/s or 8448 kbit/s.

Commercial equipment conforming to C.C.I.T.T. recommendations is now available for both first and second level multiplexes. Initially the Research Laboratories purchased sets of first level multiplexes for laboratory evaluation. A great deal of work has gone into evaluation of first level equipment and this is reported on in several other reports. Over the past three years investigations have proceeded into most aspects of secondary level multiplexing. An experimental 8448 kbits/s multiplex was developed to allow the Research Laboratories to gain an insight into the problems associated with secondary level multiplexes. Subsequently, the Research Laboratories have purchased a set of commercially made second order multiplexes for laboratory evaluation. This report describes and gives results for the tests performed on these two sets of equipment. The results show that the jitter performance of the evaluated 8448 kbit/s equipment is appreciably better than the jitter performance of the evaluated 6312 kbit/s equipment.

CONTENTS

A.J. Gibbs
for Director, Research

LIST OF TEST EQUIPMENT USED

Figures in brackets following each item correspond to the paragraph number of the test description -

1. Power Supply B.W.D. Model 246A (All tests).

2. High Speed Data Test Set. Laboratory made (4.3, 4.5.3, 4.5.4, 4.8, 4.10).

3. Pulse Generator Datapulse Model 100A (4.5.4).

4. Random Noise Generator General Radio Model 1383 (4.3.2, 4.8, 4.10).

5. Counter Hewlett-Packard Model 5245L (4.1, 4.3.2, 4.8, 4.9, 4.10, 4.11).

6. Pulse Generator (Used as a Ramp Generator). Hewlett-Packard Model 8010A (4.5.3, 4.5.4).

7. Oscilloscope, Tektronix Model 547 (4.3.1, 4.5).

8. Function Generator (Triangular Wave Generator). Tekelec Airtronic Model T.E. 500A (4.5.4).

9. Synthesiser General Radio Model 1062 (4.3, 4.5, 4.8, 4.9, 4.10, 4.11).

10. Pulse Generator, Data Dynamics Model 5102 (4.3, 4.5, 4.8, 4.9, 4.10, 4.11).

11. Memory Voltmeter. Micro Instrument Co. Model 5203 (4.5.1, 4.5.2).

12. Sinewave Oscillator, Hewlett-Packard Model 654A (4.5.2).

13. 0 - 100% Jitter Inserter, Laboratory made (4.5.1, 4.5.2).

14. 0 - 8 Bit Period Jitter Inserter, Laboratory made (4.5.3, 4.5.4).

15. Line Break Simulator/Error Inserter, Laboratory made (4.3, 4.8, 4.10).

LIST OF FIGURES

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LABORATORY TESTS ON A COMMERCIALLY AVAILABLE 6312 KBIT/S AND A COMMERCIALLY AVAILABLE 8448 KBIT/S SECOND ORDER DIGITAL MULTIPLEX

1. INTRODUCTION

The C.C.I.T.T. has made two recommendations for second order digital multiplex equipment, Rec. G.742 and G.743 (Appendix I). Commercial equipment is now available which conforms in almost all respects with the C.C.I.T.T. recommendations. The Telecom Australia Research Department has purchased second order digital multiplex equipment operating at 6312 kbit/s made by NEC, and 8448 kbit/s equipment made by GEC for laboratory evaluation. This report describes and gives results for a number of tests performed on these two sets of equipment. Where possible, the C.C.I.T.T. recommendations are used as a basis for evaluating the performance of the second order equipment.

2. BRIEF DESCRIPTION OF EACH EQUIPMENT

Both equipments use positive justification techniques to multiplex up to four plesiochronous primary PCM systems. The NEC 6312 kbit/s equipment multiplexes 1544 kbit/s data streams, and the GEC 8448 kbit/s equipment multiplexes 2048 kbit/s data streams. Both equipments operate off a supply voltage of 50 V d.c. Alarms provided on the 8448 kbit/s equipment are tributary input signal fail (at multiplexer), tributary loss of timing signal lock (at demultiplexer), line data input fail, loss of frame alignment, and power fail. Alarms provided on the 6312 kbit/s equipment are remote system alarm, 6312 kbit/s clock failure and/or out of synchronization, error in frame bit and fuse blown alarm.

3. INTRODUCTORY INFORMATION ON TESTS

All the tests performed in this report were carried out with an equipment supply voltage of 50 ± 0.5 V, and at a temperature of 20° ± 2°C. To facilitate simpler testing arrangements each equipment was modified for full width binary interface at all tributary and line connection points, with separate inputs and outputs for clock and data. Both line and tributary clock extraction circuitry were bypassed. The 8448 kbit/s equipment has internal strapping to allow this facility. The 6312 kbit/s equipment does not have this facility, and a modification was made. Where tests performed on a tributary were considered to be too time consuming to do the same test on each tributary, only one tributary was tested. An equipment warmup period of at least 4 hours was allowed before the commencement of any test.

4. DESCRIPTION AND RESULTS OF TESTS

4.1 Line Bit Rate. For both equipments the recommended tolerance on the nominal line bit rate is ± 30 parts per million.

Using a counter with an accuracy of greater than 1 part in 10^8 the line clock frequency for both equipments was measured and found to be less than ± 1 parts per million from the recommended nominal value.

4.2 Frame Structure. The frame structure of both equipments conforms to Rec. G.742 and G.743 except for the following:

In the 6312 kbit/s equipment the bits from the second and fourth tributaries are not inverted logically before multiplexing with the bits from the first and third tributaries (in this equipment a scrambler-descrambler can be strapped in series with the line data stream. The scrambler-descrambler is used as an alternative to the inversion of the second and fourth bits).

4.3 Loss and Recovery of Frame and/or Multiframe Alignment. Fig. 1 shows the test setup used for this test. The test was divided into two sections. In the first test the clock and/or data lines were interrupted or inverted for a period determined by the length of a pulse out of a pulse generator. The circuitry for controlling the line break or inversion consists basically of a gate in series with the data and/or the clock streams. This gate is opened or closed under control of the pulse fed from the pulse generator.

Only one tributary input was active in this test. Thus the chance of simulation of frame or multiframe patterns was lower than if all tributary inputs had been active. If all tributary inputs are active, maximum times given in Figs. 2 and 3 may be exceeded, with a low probability for random tributary signals.

In the second test errors were inserted onto the data stream under control of a white noise generator. The circuitry for the error inserter is identical (except for interfaces) to that shown and described in Ref. 1.

4.3.1 Line Break or Inversion Tests. This test was divided into three tests. In each test the line break time or inversion time was determined by the length of a pulse fed from a pulse generator. The tests were as follows:

(a) Data only interrupted.

(b) Data only inverted.

(c) Data and clock interrupted.

Waveforms and times associated with the tests are shown in Figs. 2 and 3. The break time was varied slightly in each test to obtain maximum and minimum times to go in and out of sync. The times were read off the oscilloscope and are shown in Figs. 2 and 3.

In the case of the 6312 kbit/s equipment test (b) (data only inverted) produced in the majority of cases waveforms as shown in Fig. 2 (b). If the data inversion period exceeded approximately 7 ms, out of sync was registered at the beginning and end of the inversion period. During the inversion period in

sync was registered. A check of the tributary output data, when in sync was registered, and with line data still inverted, revealed that the tributary output data was indeterminant during that period. The demultiplexer was therefore not in correct synchronism even though the alarm registered otherwise.

The 6312 kbit/s equipment uses a frame pattern of 0 1 per frame. A frame is repeated for four frames to form a multiframe. Inversion of the line data bits will still produce the same frame pattern except it will be displaced by one half a frame period from its correct position. The demultiplexer can therefore assume frame synchronisation in the data only inverted condition.

If the demultiplexer has assumed frame synchronisation, while in fact being half a frame out of alignment, it will commence looking for the multiframe pattern in the time slots that are occupied by the second bits of the justification codes for each tributary (see Appendix I: Frame Structure 6312 kbit/s Equipment). If the justification code bits match the multiframe code, the demultiplexer can also assume multiframe synchronisation. Waveform observation of the line data signal showed that the justification codes on the line data signal can settle on either of the two justification codes when the tributary input signal is removed. Thus the multiframe code can be simulated by a combination of the justification codes if at least three of the tributaries have no input signal. The demultiplexer would therefore assume multiframe synchronisation under these conditions.

The possibility of the line data being inverted together with the loss of input from at least three tributaries would be extremely remote. If this condition did occur in practice no alarms would be registered and incorrect tributary output information would be transmitted.

In the case of the 8448 kbit/s equipment the average time to register out of sync in tests (a) and (b) corresponded to an average of 3.5 frame periods which is in agreement with Rec. G742. The average time to register in sync corresponded to an average of 1.5 frame periods.

4.3.2 Error Performance. The test setup shown in Fig. 1 for error performance was used in this test.

For the 8448 kbit/s equipment the error rate inserted on to the line data stream was increased, with an observing time of a few seconds after each increase, until the first occurrence of the loss of frame alignment alarm. All the errors inserted were recorded on the counter and thus the error rate could be calculated. A number of error rates were recorded and an average error rate calculated. The results showed that the line error rate had to be in the vicinity of 1 error in 1.2×10^2 bits before the loss of frame alignment alarm was registered within a few seconds.

Using the same method for the 6312 kbit/s equipment as just outlined, and noting the first occurrance of the loss of synchronization alarm, the results showed that the line error rate had to be in the vicinity of 1 error in 2.7×10^2 bits. For line errors to have any effect on the error-in-frame-bit alarm the line error rate had to be in the vicinity of 1 error in 1.7×10^4 bits.

4.4 Multiplexing Method. Both sets of equipment conform to Rec. G.742 and G.743 in this respect.

In the case of the 6312 kbit/s equipment it could not be ascertained from the handbooks whether majority decision is used in the detection of the justification codes, but results given in section 4.8 indicate that majority decision is used.

4.5 Jitter. The series of tests performed under this heading took up most of the time allocated to the test programme. Rec. G.742 and G.743 give no recommendations on jitter apart from recommending that this subject be studied. A number of different tests were performed:

(i) Output tributary jitter with no input jitter.

(ii) Output tributary jitter with input jitter.

(iii) Jitter Tolerance of tributary input buffer.

(iv) Jitter Tolerance of tributary output buffer.

Tests (i) and (ii) were performed with the aid of two specialised items of equipment designed and constructed for jitter measurements on a 8448 kbit/s +/0/- multiplex as described in Ref. 1 & 2.

The first item is a peak-to-peak (p - p) jitter measuring set and is described in reference 2. The second item is a 0 - 1 bit period jitter insertor which operates similarly as the first stage of a 0 - 8 bit period jitter insertor described in Appendix II. This 0 - 8 bit period jitter insertor was designed and constructed for tests (iii) and (iv), its operation is fully described in Appendix II.

For tests (i) and (ii) the output jitter was measured using either the p - p jitter measuring set, or an oscilloscope triggered off the reference clock. Only where it was difficult to see the extremities of jitter on the oscilloscope (e.g. when measuring gaussian type jitter) was the p - p jitter measuring set used.

For multiplex jitter measurements the difference Δ between the tributary input clock frequency and the multiplex reading clock (the clock which "reads" the information out of the input buffer) frequency determines the jitter performance. Therefore measurements were made of the output jitter as a function of this frequency difference Δ.

In test (i) and (ii) the frequency of the reading clock was measured each day with an accuracy of 1 part in 10^8 before the commencement of any tests. The difference between the measured

reading clock frequency and the nominal reading clock frequency was transferred as an adjustment to the selected frequency of the synthesiser used to generate tributary input data in the tests. The normal operating range for 6312 kbit/s equipment is $\Delta = \pm 120$ Hz, whereas for 8448 kbit/s equipment this figure is $\Delta = \pm 160$ Hz.

In assessing the output tributary jitter it is important to know the 3 dB cut-off point of the Phase Locked Loop (P.L.L.) used to smooth the output signals (the P.L.L. acts as a low pass filter, see also paragraph 4.5.4). This cut-off was measured as:

6312 kbit/s equipment - 40 Hz
8448 kbit/s equipment - 35 Hz

4.5.1 Output Tributary Jitter with No Input Jitter. Fig. 4 shows the test setup for this test. Results are given in Figs. 5 & 6. As shown, performance of the 8448 kbit/s equipment is better than for the 6312 kbit/s equipment.

4.5.2 Output Tributary Jitter with Input Jitter. Fig. 4 shows the test setup for this test. Results are given in Figs. 7 to 16. The "peak-to-peak" ("p - p") gaussian jitter is defined here as the 99.7% probability level.

4.5.3 Jitter Tolerance of Tributary Input Buffer. In justification systems the tributary input data stream is written into an elastic buffer and read out using a clock which has nominally the same frequency as the writing clock. The justification process ensures that on average the read clock has the same frequency as the write clock. The buffer is usually designed to have some spare capacity to allow for the effect of input jitter. Ref.3 shows the relationship between input jitter and required tributary input buffer capacity.

A Pseudo Random Binary Sequence (P.R.B.S.) data stream was fed into the input of the tributary input buffer. Data and clock at the output of the buffer were fed into a P.R.B.S. error detector. The required buffer spare capacity is determined by the phase change rate of the input signal and by the available justification capacity. Therefore, triangular wave jitter at various frequencies was introduced onto the input clock of the buffer. Fig. 17 shows the test setup. For any jitter frequency, the point at which data errors occurred through the buffer was taken to be the maximum jitter that the input buffer could take at the frequency. The jitter amplitude was measured using an oscilloscope triggered off the unjittered clock. Results of this test are given in Fig. 18.

4.5.4 Jitter Tolerance of Tributary Output Buffer. In justification systems the demultiplexed tributary data stream is written into an elastic buffer using a clock which has a large amount of multiplex jitter. The multiplex jitter has high frequency components and may also consist of low frequency components caused by the justification process.

In most systems a Phase-Locked Loop (P.L.L.) derived clock is locked onto the write clock, and is used to read data out of the buffer. The cut-off point of the P.L.L. is designed to be at a low frequency, which will attenuate any high frequency jitter from the write clock. Low frequency multiplex jitter components will not be attenuated. The buffer is usually designed to absorb the multiplex jitter and to have some spare capacity to allow for the absorption of jitter outside the passband of the P.L.L. such as jitter on the multiplexed line and jitter due to tributary input jitter.

The purpose of this test is to determine the jitter tolerance of the tributiary output buffer.

There are a number of methods of determining the jitter tolerance of the tributary output buffer and they are described briefly below.

(a) Inserting jitter on the multiplexed line.

This is the simplest way to measure the output buffer jitter tolerance provided the jitter frequency is somewhat higher than the P.L.L. cut-off point. The only constraint is that a large amount of jitter would need to be inserted onto the line before it would have any effect on the output buffer. It was known that the 8448 kbit/s equipment has a spare buffer capacity of approximately 6 bits. Thus 6 x 4 = 24 bits of jitter would need to be inserted onto the line before it would have any effect on the output buffer.

(b) Inserting jitter on the write clock of the output buffer.

This method also has the disadvantage that the capacity of the jitter inserter has to be large.

In the 8448 kbit/s equipment the write clock has inherent jitter of approximately 3 - 4 bits, and the output buffer has a spare capacity of approximately 6 bits. Any jitter on the input to the jitter inserter will be transferred directly to the output, and will proportionally reduce the ability to insert additional jitter by the jitter inserter. Thus in this case only 8 - (3-4) or 4 - 5 bits can be inserted by the jitter inserter, and this would not be enough for a spare capacity of 6 bits.

(c) Breaking the P.L.L. feedback loop and using an external jittery clock (locked to the tributary input clock) as the read clock of the elastic memory.

The test setup for this method is shown in Fig. 19. This method appeared to be very suitable. The phase of the clock fed into the jitter inserter could be shifted relative to the tributary input clock by means of the pulse generator feeding into the jitter inserter. Thus the clock out of the jitter inserter which was used as the read clock for the elastic memory, can also be phase shifted relative to the write clock of the elastic memory. The phase differences between the read and write clocks were noted before the P.L.L. feedback loop was broken. The position of the new read clock was then adjusted to give the same phase differences as before.

The jitter was then inserted and increased until data errors occurred through the system. The frequency of the jitter is not particularly important in this test.

Because the phase differences between the read and write clocks using the P.L.L. setup changes slightly for various tributary input frequencies, the output buffer jitter tolerance was measured at three different tributary input frequencies i.e. nominal, + 150 Hz and - 150 Hz from nominal.

Results of measurements

TABLE 1

Tributary Input Frequency	Maximum Jitter Tolerance in Tributary Bit Periods	
	6312 kbit/s Equipment	8448 kbit/s Equipment
Nominal	≃2.5	≃4.6
- 150 Hz from Nominal	≃1.4	≃4.4
+ 150 Hz from Nominal	≃1.0	≃5.0

4.6 Digital Interfaces

(i) 6312 kbit/s Equipment:

Both tributary and line inputs and outputs are interfaced at an impedance of 110 ohms, balanced, and with an A.M.I. pulse code of 50% duty cycle.

(ii) 8448 kbit/s Equipment:

Both tributary and line inputs and outputs are interfaced at an impedance of 75 ohms, unbalanced, and with a HDB3 line code of 50% duty cycle.

4.7 External Timing Signal. Both systems can be strapped to accept an external multiplexer timing signal.

4.8 Error Sensitivity of Justification. The test setup shown in Fig. 1 for error performance was used in this test. If the error rate on the line signal is high enough for the justification detection circuitry to misinterpret a justification code, the effect will be that a slip in the tributary clock will occur. This can be measured on the P.R.B.S. Detector by loss of synchronization occuring. On the P.R.B.S. Detector used for this test, loss of synchronization can be noted by a sudden increase in the errors detected.

The line error rate was increased slowly until a sudden increase in the errors detected in the tributary output signal was noted. This was taken to be the point at which slip occurred

due to a misinterpretation of a justification code. The line error rate was then calculated. The test was repeated a number of times to obtain an average line error rate.

Results

TABLE 2

Equipment	Average line error rate required to cause incorrect detection of justification code within a few seconds
6312 kbit/s	6.2×10^2 bits/error
8448 kbit/s	6.5×10^2 bits/error

4.9 Justification Margin of Multiplex. As explained in Section 4.5.4 most justification systems use a P.L.L. derived clock to read data out of the receive buffer. Because the tracking range of the P.L.L. is generally much smaller than the maximum justification capacity of the system, the allowable deviation of the input tributary clock is generally limited by the tracking range of the P.L.L.

The purpose of this test is to determine the tracking range of the P.L.L.'s in the two systems.

The same test setup as shown in Fig. 1 was used for this test except that the line signal was not subject to line breaks or errors. All four tributaries were measured.

Results

TABLE 3

Equipment	Deviation of Input Tributary Clock from Nominal before tributary output errors occur. (Minimum values out of four Tributaries)
6312 kbit/s	+ 230 Hz from nominal - 260 Hz from nominal
8448 kbit/s	+ 510 Hz from nominal - 270 Hz from nominal

4.10 Ratio of Line Error Rate/Tributary Output Error Rate. The test setup for this test is as shown in Fig. 1 for error performance.

The line error rate was set to between 1 in 10^4 and 1 in 10^5 bits/error to ensure that line errors would not initiate any alarms or cause errors in the justification process. The tributary output error rate during the measuring period was then measured. This procedure was repeated a number of times and an average line and tributary error rate calculated.

Under ideal measuring conditions the ratio between the line error rate and tributary output error rate should be 1:1. The results of the measurements taken in this test showed that both systems gave results very close to the ideal ratio.

4.11 Free Running Tributary Output Rate. This test was divided into two sections,

(i) Free running tributary output rate when there is a system alarm.

(ii) Free running tributary output rate when there is no tributary input clock signal.

The same counter as described in Section 4.1 was used for measurement of the tributary clock frequencies.

Results

TABLE 4

Equipment	Test (i)	Test (ii)
6312 kbit/s	No clock signal Note 1	No clock signal Note 2
8448 kbit/s	Out of four tributaries max. dev. from nominal 37 Hz (19 ppm). Note 3	Max. dev. from nominal 5 Hz (3 ppm) Note 4

Notes

1. As shown in Fig. 2 the tributary outputs are clamped to the "low" state during out of synchronisation alarm conditions. The other two demultiplex alarms (6312 kbit/s clock failure and error in frame bit) also clamp the tributary outputs to the low state. In normal operation the tributary output is a bipolar A.M.I. type signal. Under alarm conditions the tributary output would be all zeros thus conveying no information of the tributary output clock rate. For this reason no measurements were taken of the tributary output clock rate in test (i).

2. If the bipolar tributary input is removed the internal clock extraction takes a finite time to "die" away. This has the effect of still clocking tributary input data for a short period after the removal of the tributary input. Therefore, loss of tributary input is equivalent to all zeros input. This will be propagated to the tributary output, thus giving all zero tributary output and no information of the tributary output clock rate.

3. In the 8448 kbit/s equipment the tributary outputs are HDB3 coded. During demultiplexer alarm conditions the tributary binary outputs are clamped to all zeros which is passed through HDB3 convertor to provide a one for every three zeros in the signal output. The alarm conditions also initiate a clamp to restrict the tributary output bit rate.

4. Under loss of tributary input conditions a detector switches in a standby 2048 kbit/s oscillator as a subsititue clock. This action serves to maintain the receive tributary oscillator at its correct frequency.

5. CONCLUSIONS

The results of a series of measurements on a 6312 kbit/s and a 8448 kbit/s second order digital multiplex have been recorded in this report.

As yet, no standards for jitter performance have been drafted by the C.C.I.T.T. In comparing the two sets of equipment, it is evident that the jitter performance of the 8448 kbit/s equipment is appreciably better than the jitter performance of the 6312 kbit/s equipment. It is thought that the better jitter performance of the 8448 kbit/s equipment is largely due to its larger justification capacity as compared with the 6312 kbit/s equipment.

The alarm and monitor facilities of the GEC multiplex are more extensive than for the NEC multiplex. The NEC multiplex does not provide any tributary alarms such as loss of tributary input signal or provide a tributary output signal with a timing component during multiplex alarm condition. An evaluation would be required to determine the required alarm and monitor facilities in practical operation.

The frame and multiframe signals in the 8448 kbit/s equipment allow a faster and more stable frame alignment system than is possible with the 6312 kbit/s equipment. Whether this is of practical significance would require further study. In particular, empirical out-of-frame alignment statistics would be required.

ACKNOWLEDGEMENT

The author wishes to thank Mr. J. Carrol for performing some of the measurements, and Mr. J.A. Bylstra for his assistance in preparation of the report and general guidance with the measurement program.

REFERENCES

1. J.A. Bylstra, "Laboratory Evaluation on Case 670 and Timeplex T-20 data multiplex equipment". R.L. Report No. 7035.

2. C.C.I.T.T., Com. Special D, "Results of Measurements of Jitter due to Justification in Digital Multiplexes". Doc No. 167, January 1975.

3. C.C.I.T.T., Com. Special D, "Impact of Jitter on the Second Order Digital Multiplex at 6.312 Mb/s". Doc No. 5, 8-12 November 1971.

APPENDIX II

A 0-8 Bit Period Jitter Inserter

This equipment was designed and constructed specifically for use in two tests reported on in this report. Because the equipment may have application in other fields a description of its operation is given here. Refer to circuit diagram 1.

An unjittered clock is fed into the "Clock In" connector. The signal from the "$\frac{\text{clock}}{8}$ out" connector is used to trigger a ramp generator. The ramp is fed into the "Ramp In" connector and must have a polarity as shown on the circuit diagram. With no signal applied to the "Noise In" connector the comparator will switch about the a.c. zero points of the incoming ramp waveform generating a square wave at its output. The trailing edge of the square wave corresponds to the trailing edge of the ramp. Monostable 1 triggers on the leading edge of the square wave out of the comparator, and is timed to produce a pulse having a duration of one half the period of the ramp.

If a jitter modulating signal is introduced into the "Noise In" connector, the point at which the comparator switches is determined by the relative levels of the jitter modulating signal and the ramp waveform. It can be seen that the level of the jitter modulating signal will only affect the switching point of the comparator during the rising portion of the ramp waveform. The comparator could therefore switch at positions up to ± 180° from the centre of the ramp depending on the instantaneous amplitude of the jitter modulating signal. Jitter of up to 8 clock periods at the original clock rate can therefore be inserted onto the square wave generated by monostable 1, remembering that this square wave is at a rate of one eighth the original clock rate.

Monostables 2 to 4 together with associated components, multiply the output of monostable 1 by eight with each monostable functioning as a multiply by two stage. To function as multiply by two stages, monostables 2 to 4 must trigger on both edges of the square wave fed from their respective preceding stages. This is achieved by differentiating the output of each preceding stages of monostables 2 to 4 and adding the two differentiated outputs together in an exclusive or gate. Each monostable is timed to produce a pulse having a duration of one half the width of the preceding monostable. Thus if monostable 1 has a duration of one half the period of the ramp (4 clock periods), then monostable 4 will have a duration of one sixteenth of the period of the ramp (half a clock period).

The amount of jitter inserted can be monitored using an oscilloscope triggered off the original unjittered clock.

The pulse width out of each monostable can be adjusted over a small range by potentiometers as shown on the circuit diagram.

As shown in Fig. 18 the maximum amount of jitter that the jitter insertor can produce reduces as the jitter frequency increases. Refer to Ref. 2 for further information on the jitter frequency limits of this jitter insertor.

Recommendation G.742 (Geneva, 1972)

SECOND ORDER DIGITAL MULTIPLEX EQUIPMENT OPERATING AT 8448 kbit/s AND USING POSITIVE JUSTIFICATION

1. *General*

The second order digital multiplex equipment using positive justification, described below, is intended for use on digital paths between countries using 2048 kbit/s primary multiplex equipments such as the PCM multiplex equipment according to Recommendation G.732.

2. *Bit rate*

The nominal bit rate should be 8448 kbit/s.

The tolerance on that rate should be ±30 parts per million (ppm).

3. *Frame structure*

Table 1 gives:

— the tributary bit rate and the number of tributaries;
— the number of bits per frame;
— the bit numbering scheme;
— the bit assignment;
— the bunched frame alignment signal.

4. *Loss and recovery of frame alignment and consequent action*

Loss of frame alignment should be assumed to have taken place when four consecutive frame alignment signals have been incorrectly received in their predicted positions.

When frame alignment is assumed to be lost, the frame alignment device should decide that such alignment has effectively been recovered when it detects the presence of three consecutive frame alignment signals.

The frame alignment device having detected the appearance of a single correct frame alignment signal, should begin a new search for the frame alignment signal when it detects the absence of the frame alignment signal in one of the two following frames.

Note. — As it is not strictly necessary to specify the detailed frame alignment strategy, any suitable frame alignment strategy may be used provided the performance achieved is at least as efficient in all respects as that obtained by the above frame alignment strategy.

As soon as frame alignment has been lost and until it has been recovered, a definite pattern should be sent on all tributaries at the output of the demultiplexer. The pattern is under study.

5. *Multiplexing method*

Cyclic bit interleaving in the tributary numbering order and positive justification is recommended.

The justification control signal should be distributed and use the C_{jn} — bits ($n = 1, 2, 3$, see Table 1).

Positive justification should be indicated by the signal 111, no justification by the signal 000. Majority decision is recommended.

Table 1 gives the maximum justification rate per tributary and the ratio of the maximum justification rate to the nominal justification rate.

6. *Jitter*

The amount of jitter that should be accepted at the input of the multiplexer and at the input of the demultiplexer, as well as the amount of jitter at the output of the demultiplexer, should be studied and specified.

7. *Digital interfaces*

Under study.

8. *Timing signal*

If it is economically feasible, it may be desirable to be able to derive the multiplexer timing signal from an external source as well as from an internal source.

9. *Service digits*

Two bits per frame are available for service functions. Bit 11 of Set I is used to transmit an alarm when a fault condition occurs in the multiplex equipment (such as loss of frame alignment). Bit 11 of Set I has the value "0" when there is no fault condition and the value "1" when a fault condition occurs. Bit 12 of Set I is reserved for national use. On the digital path crossing the border, this bit is fixed at "1".

TABLE 1

Frame structure	Bit numbering scheme
Tributary bit rate (kbit/s)	2048
Number of tributaries	4
	Set I
Frame alignment signal (1111010000)	1 to 10
Bit used for international transmission of alarms	11
Bit reserved for national use	12
Bits from tributaries	13 to 212
	Set II
Justification control bits C_{j1} (see note)	1 to 4
Bits from tributaries	5 to 212
	Set III
Justification control bits C_{j2} (see note)	1 to 4
Bits from tributaries	5 to 212
	Set IV
Justification control bits C_{j3} (see note)	1 to 4
Bits from tributaries available for justification	5 to 8
Bits from tributaries	9 to 212
Frame length	848 bits
Bits per tributary	206 bits
Maximum justification rate per tributary	10 kbit/s
Maximum justification rate/nominal justification rate	2.36

Note. — C_{ji} indicates the ith justification control bit of the jth tributary.

Recommendation G.743 (Geneva, 1972)

SECOND ORDER DIGITAL MULTIPLEX EQUIPMENT OPERATING AT 6312 kbit/s AND USING POSITIVE JUSTIFICATION

1. *General*

The second order digital multiplex equipment using positive justification described below, is intended for use on digital paths between countries using 1544 kbit/s primary multiplex equipments such as the PCM multiplex equipment according to Recommendation G.733.

2. *Bit rate*

The nominal bit rate should be 6312 kbit/s.

The tolerance on that rate should be ±30 parts per million (ppm).

3. *Frame structure*

Table 1 gives:

— the tributary bit rate and the number of tributaries;
— the number of bits per frame;
— the bit numbering scheme;
— the bit assignment;
— the distributed frame and multiframe alignment signals.

4. *Loss and recovery of frame and multiframe alignment and consequent action*

The frame alignment recovery time should not exceed 16 ms. The signal to be applied to the tributaries during the out-of-frame-alignment time should be studied.

Once frame alignment is established, multiframe alignment should be recovered in less than 420 microseconds.

5. *Multiplexing method*

Cyclic bit interleaving in the tributary numbering order and positive justification is recommended.

The justification control signal should be distributed and use the C_{jn} — bits ($n = 1, 2, 3$, see Table 1).

Positive justification should be indicated by the signal 111, no justification by the signal 000. Majority decision is recommended.

Table 1 gives the maximum justification rate per tributary and the ratio of the maximum justification rate to the nominal justification rate.

6. *Jitter*

The amount of jitter that should be accepted at the input of the multiplexer and at the input of the demultiplexer, as well as the amount of jitter at the output of the demultiplexer, should be studied and specified.

7. *Digital interfaces*

Under study.

8. *Timing signal*

If it is economically feasible, it may be desirable to be able to derive the multiplexer timing signal from an external source as well as from an internal source.

9. *Service digits*

Under study.

TABLE 1

Tributary bit rate (kbit/s)	1544
Number of tributaries	4
Frame structure (Notes 1 and 4)	**Bit numbering scheme**
	Set I
Bit for multiframe alignment signal (M_j) (Note 1)	1
Bits from tributaries	2 to 49
	Set II
1st bit for justification control signal (C_{j1})	1
Bits from tributaries	2 to 49
	Set III
1st bit for frame alignment signal (F_0) (Note 3)	1
Bits from tributaries	2 to 49
	Set IV
2nd bit for justification control signal (C_{j2})	1
Bits from tributaries	2 to 49
	Set V
3rd bit for justification control signal (C_{j3})	1
Bits from tributaries	2 to 49
	Set VI
2nd bit for frame alignment signal (F_1) (Note 3)	1
Bits from tributaries (Note 2)	2 to 49
Frame length	294 bits
Multiframe length	1176 bits
Bits per tributary per multiframe (including justification)	288 bits
Maximum justification rate per tributary	5367 kbit/s
Maximum justification rate/nominal justification rate	2.99

Note 1. — This frame is repeated 4 times to form a multiframe with frames designated $g = 1, 2, 3, 4$. The multiframe alignment signal is a 011x-pattern. x may be used as an alarm service digit.

Note 2. — The bit available for the justification of tributary j is the first time slot of tributary j following F_1 in the in the jth frame.

Note 3. — The frame alignment signal is $F_0 = 0$ and $F_1 = 1$.

Note 4. — The bits from the second and fourth tributaries are inverted logically before multiplexing with the bits from the first and third tributaries.

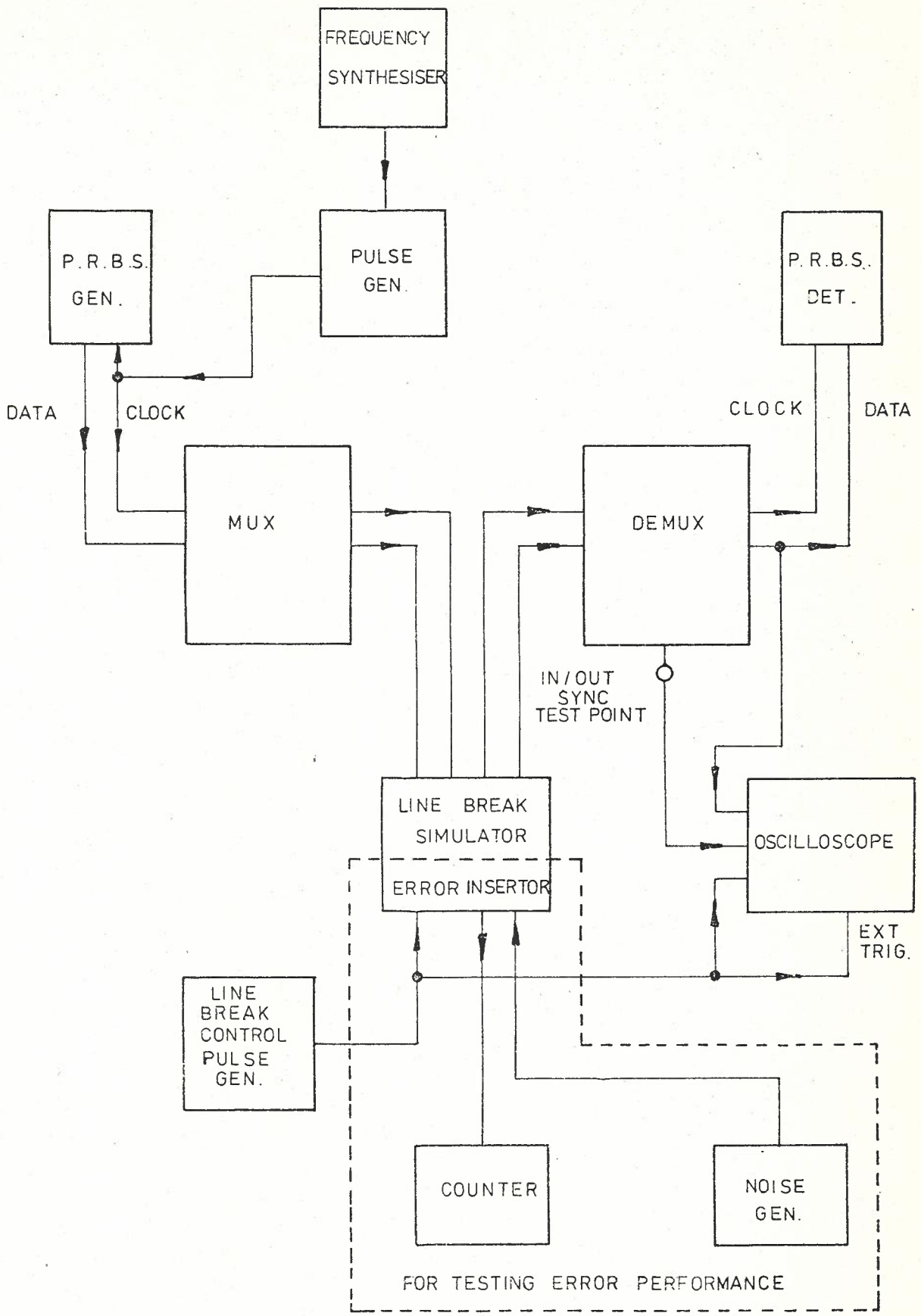
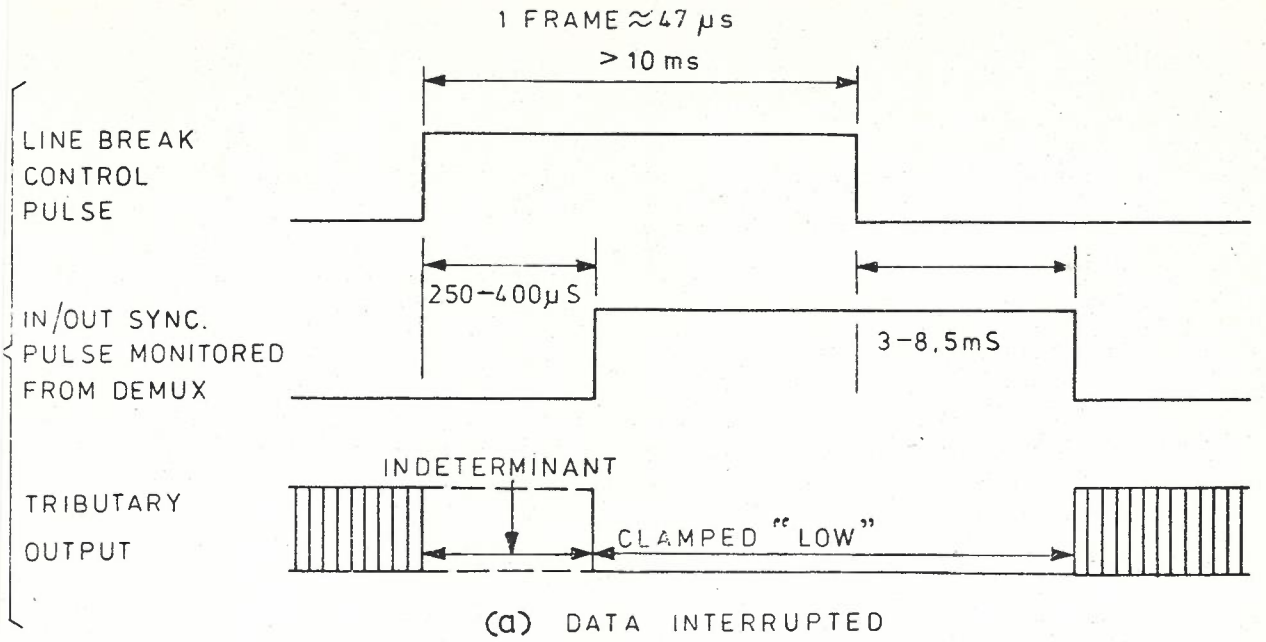
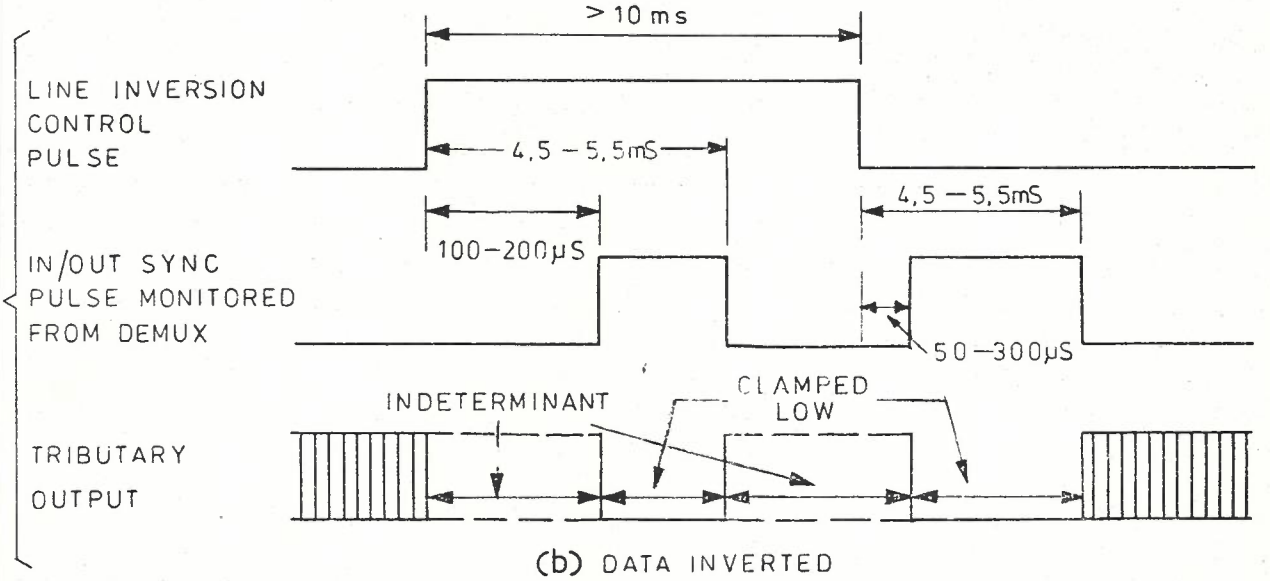


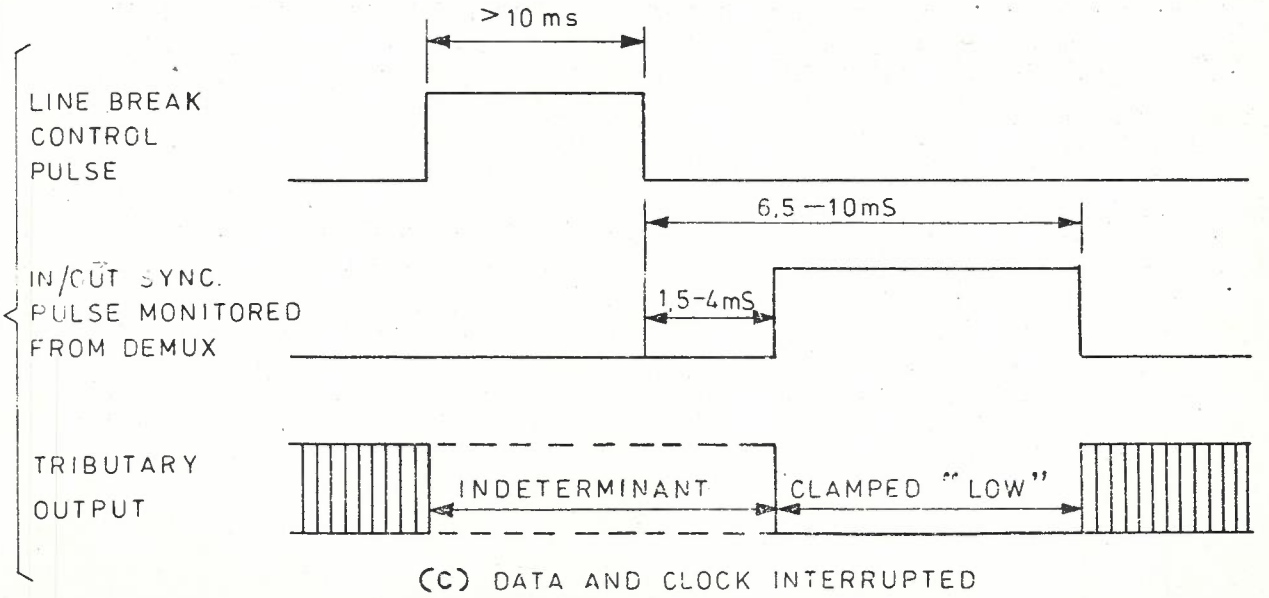
FIG. 1. TEST SETUP FOR MEASUREMENT OF FRAMING AND ERROR PERFORMANCE



(a) DATA INTERRUPTED



(b) DATA INVERTED



(c) DATA AND CLOCK INTERRUPTED

FIG. 2 6312 k bit/s SYSTEM – WAVEFORMS ASSOCIATED WITH FRAMING PERFORMANCE.

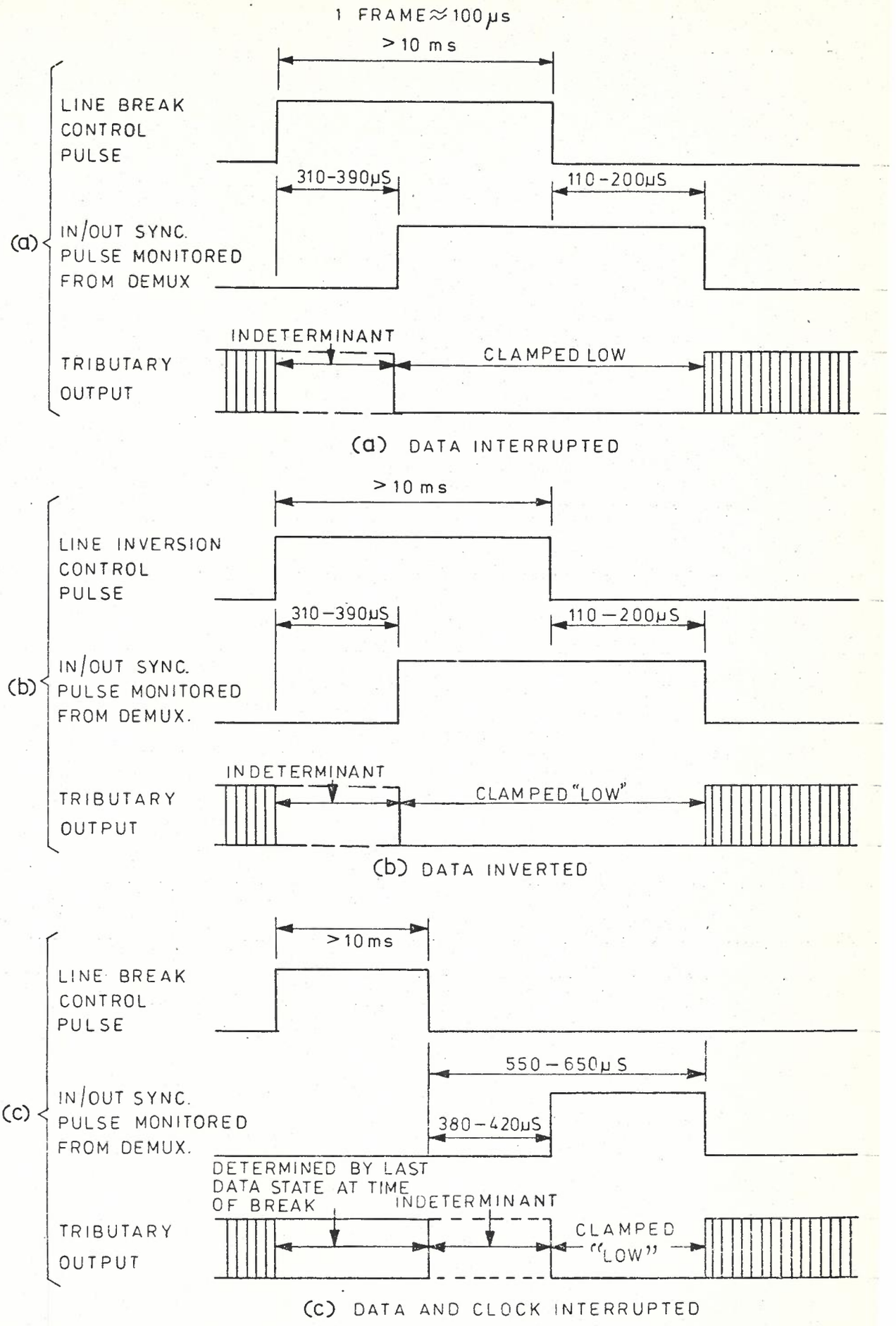


FIG. 3 8448 kbit/s SYSTEM—WAVEFORMS ASSOCIATED WITH FRAMING PERFORMANCE.

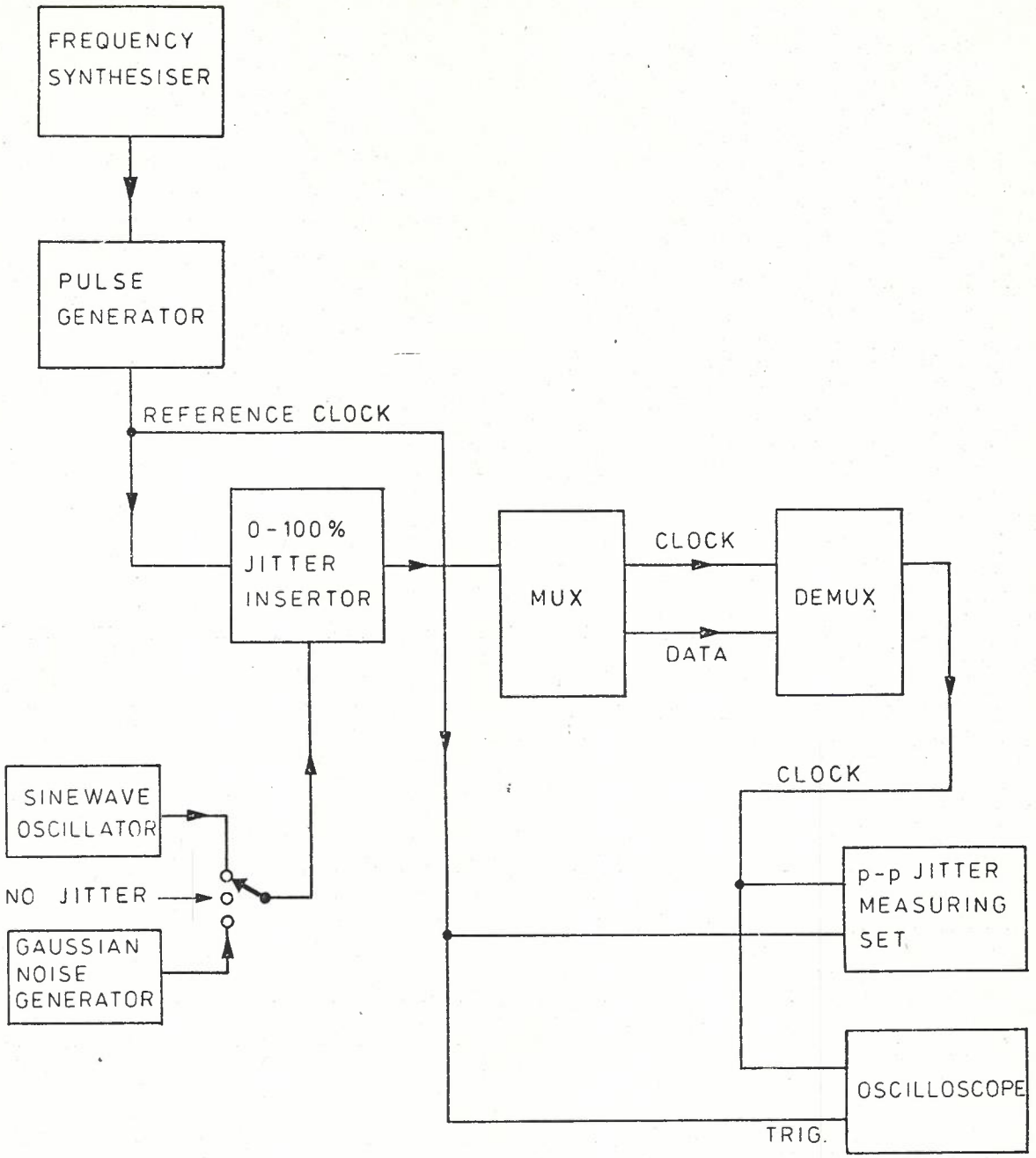


FIG. 4 TEST SETUP FOR MEASUREMENT OF TRIBUTARY OUTPUT JITTER.

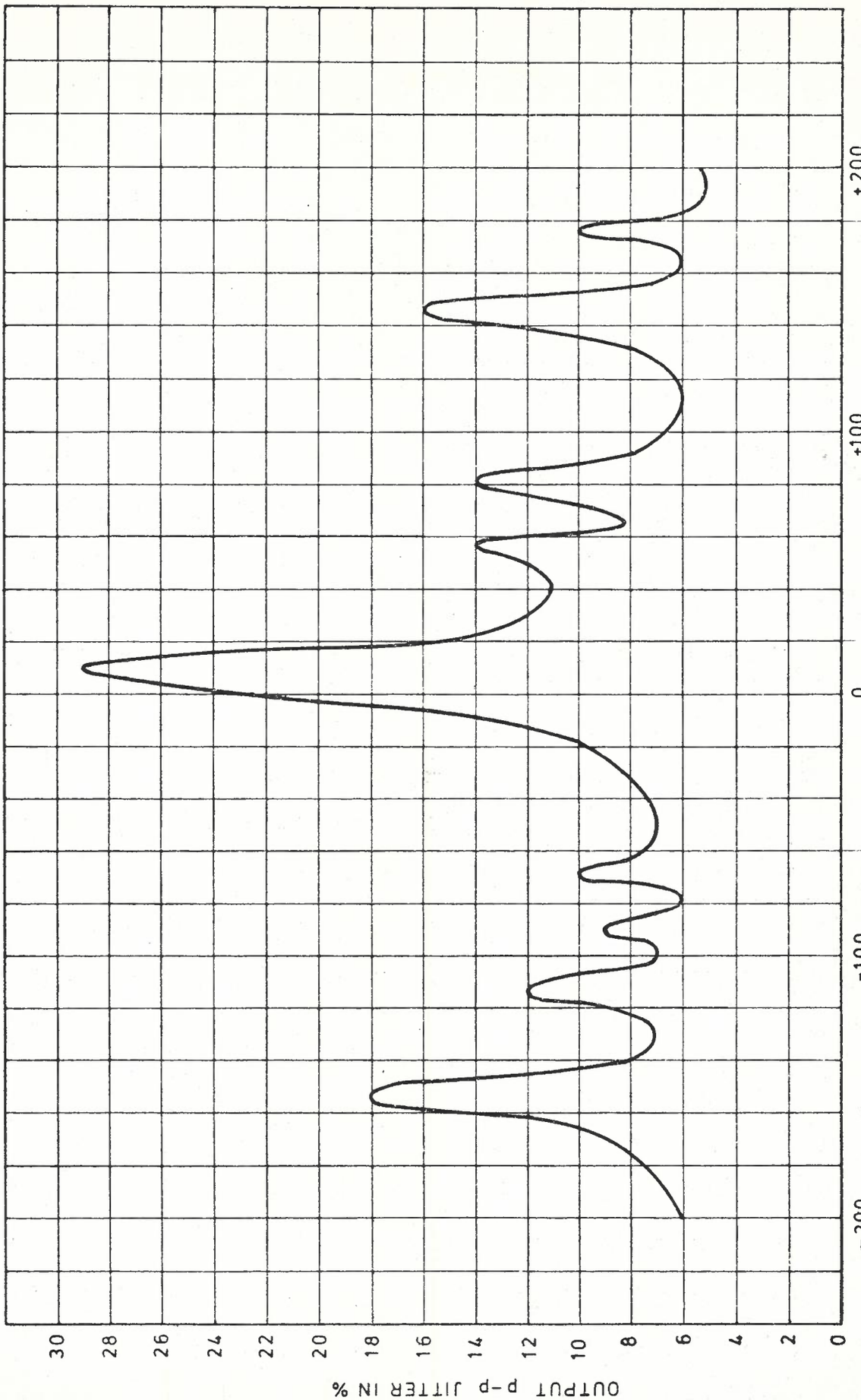


FIG. 5 MEASURED OUTPUT JITTER OF 6312 kbit/s SYSTEM WITH NO INPUT TRIBUTARY JITTER.

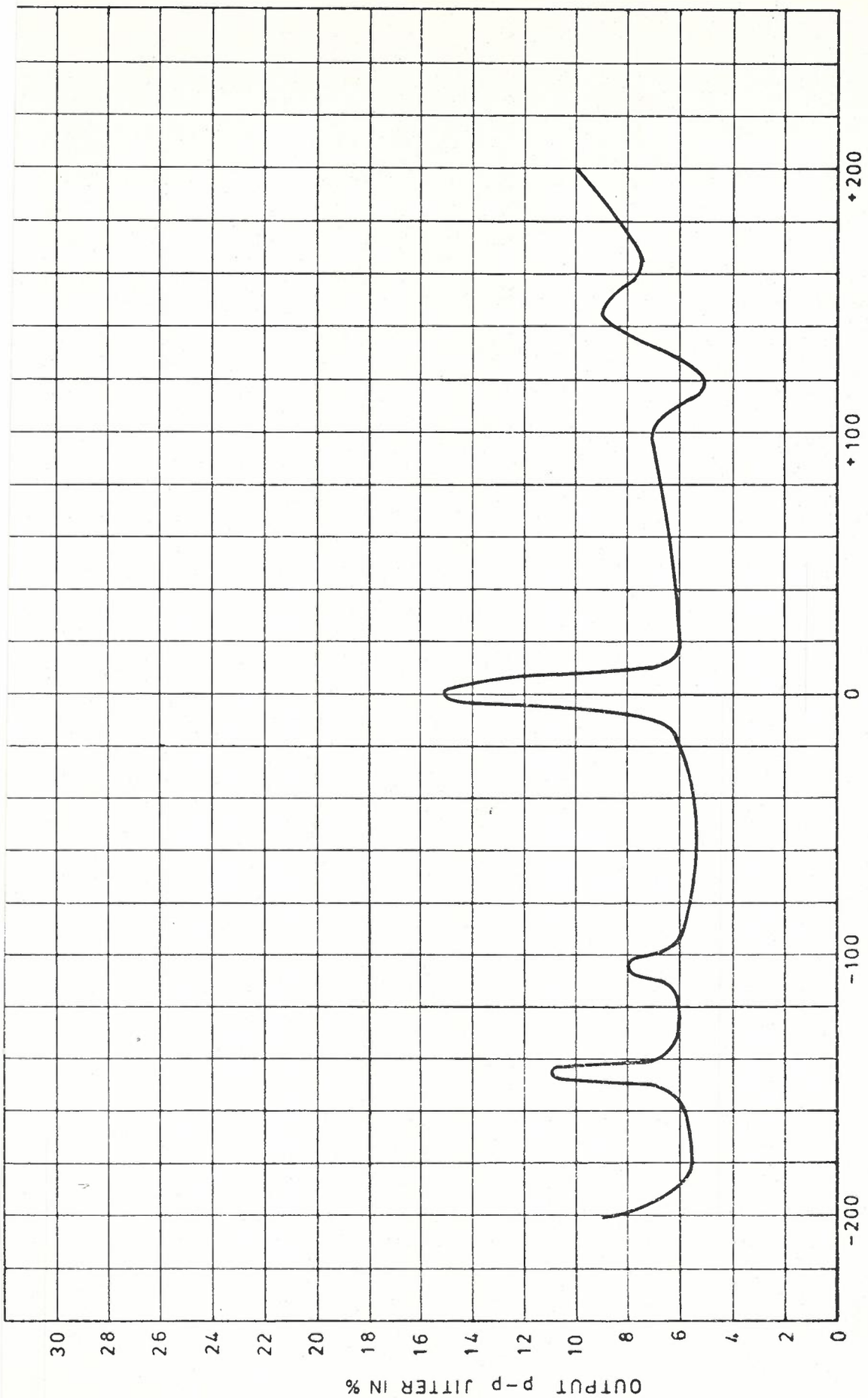


FIG. 6 MEASURED OUTPUT JITTER OF 8448 kbit/s SYSTEM WITH NO INPUT TRIBUTARY JITTER.

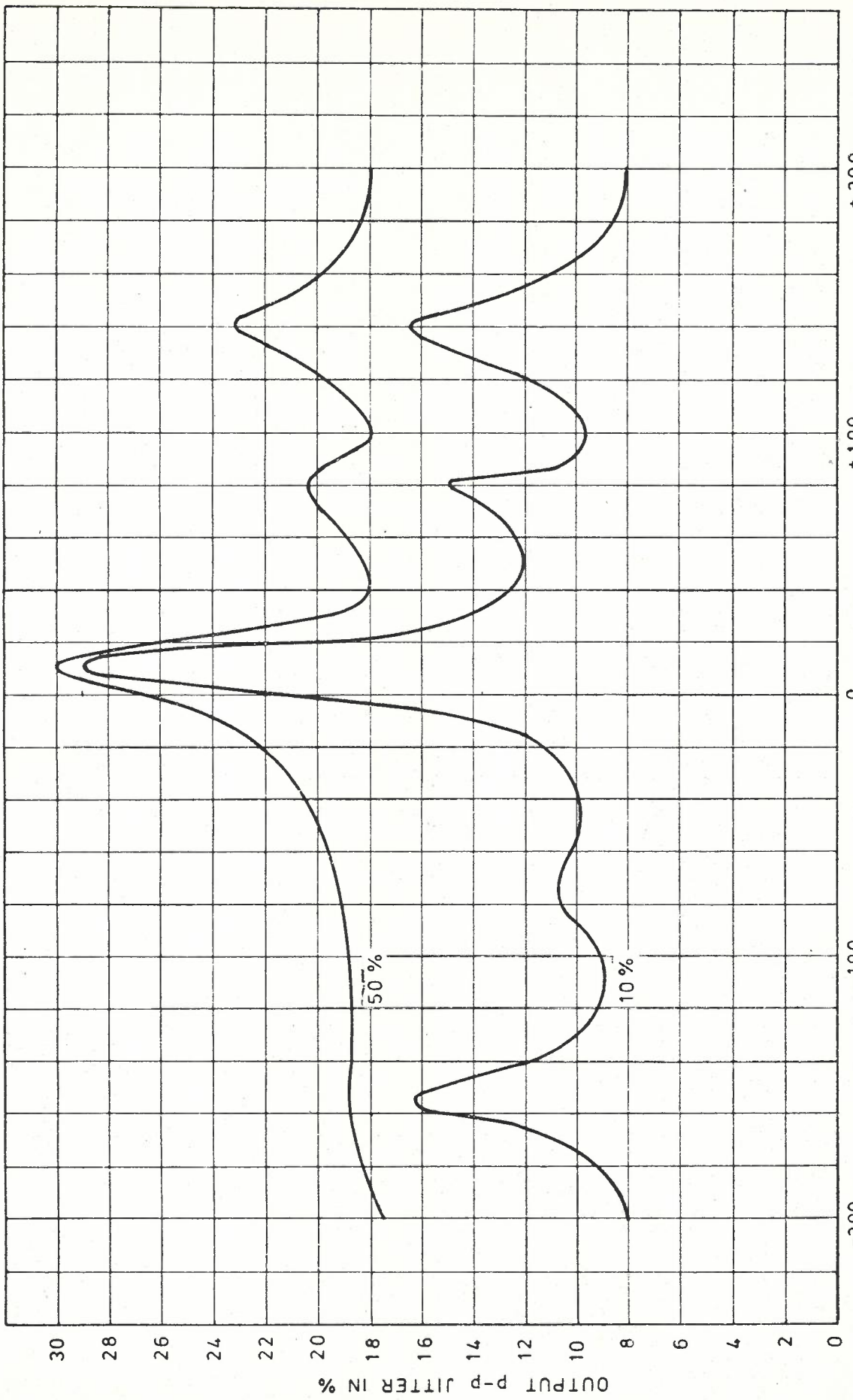


FIG. 7 MEASURED OUTPUT JITTER OF 6312 kbit/s SYSTEM WITH 10 % AND 50 % "p-p" GAUSSIAN INPUT TRIBUTARY JITTER.

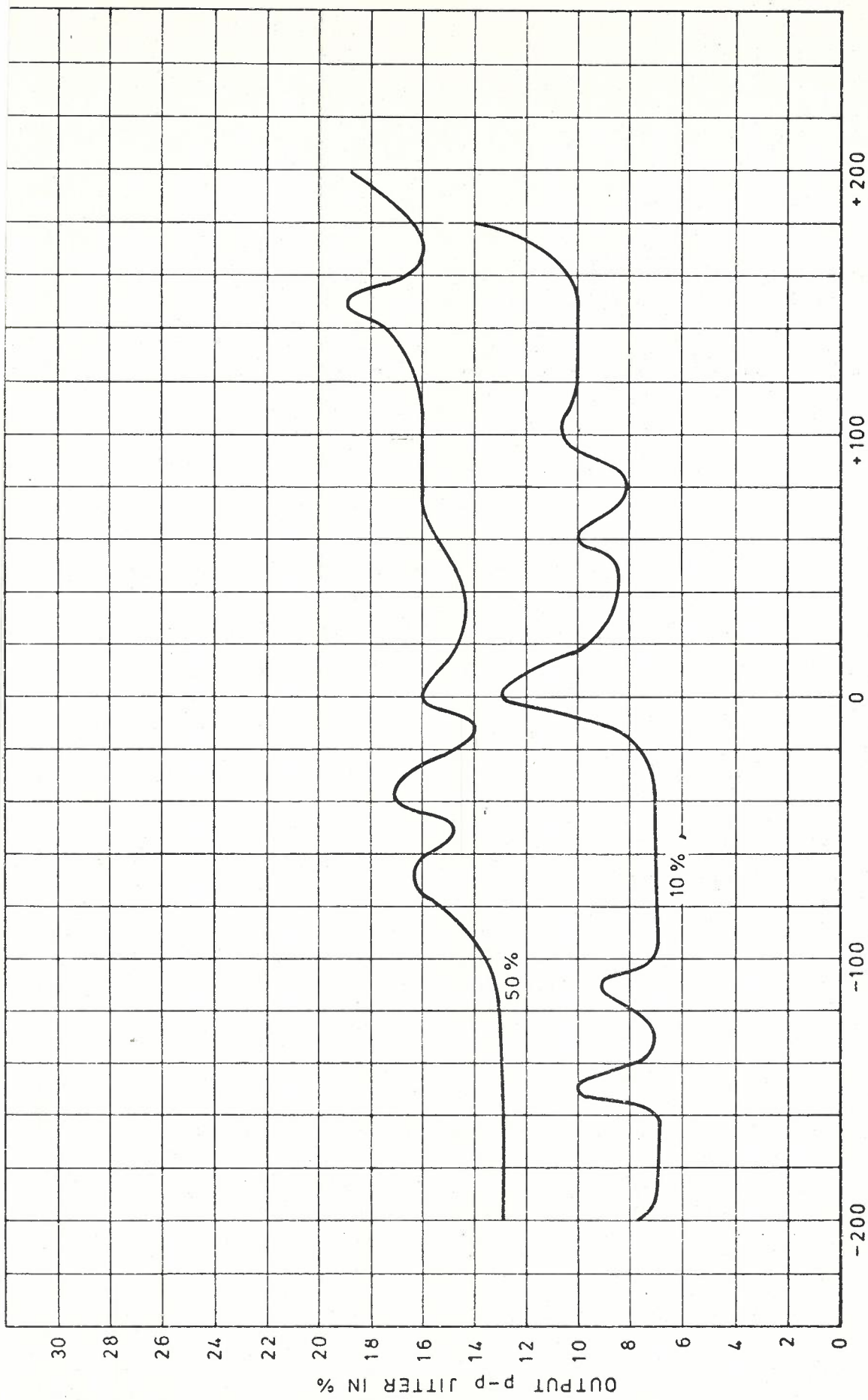


FIG. 8 MEASURED OUTPUT JITTER OF 8448 kbit/s SYSTEM WITH 10 % AND 50 % "p-p" GAUSSIAN INPUT TRIBUTARY JITTER.

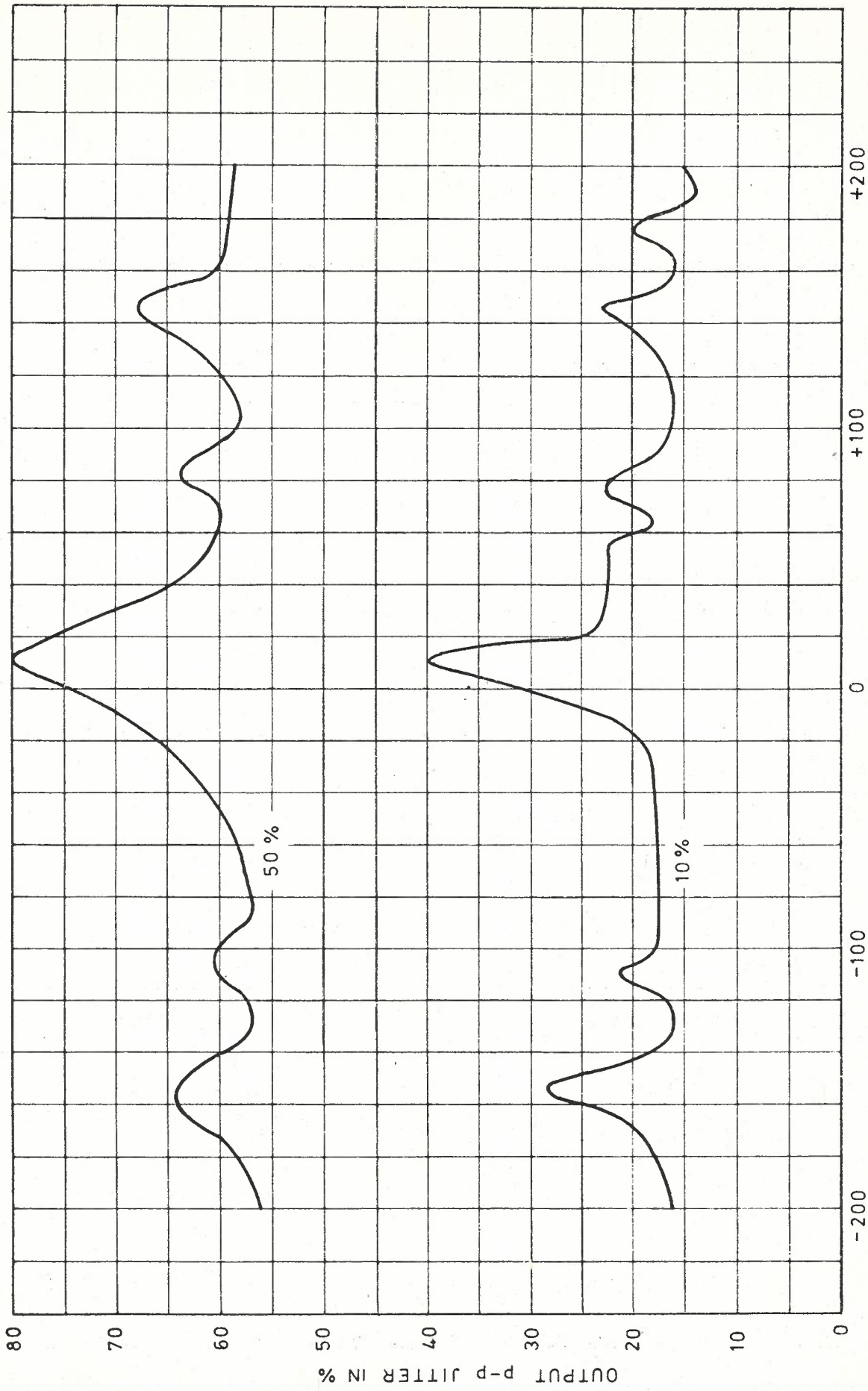


FIG. 9 MEASURED OUTPUT JITTER OF 6312 kbit/s SYSTEM WITH 10% AND 50% p-p 10Hz SINEWAVE INPUT TRIBUTARY JITTER

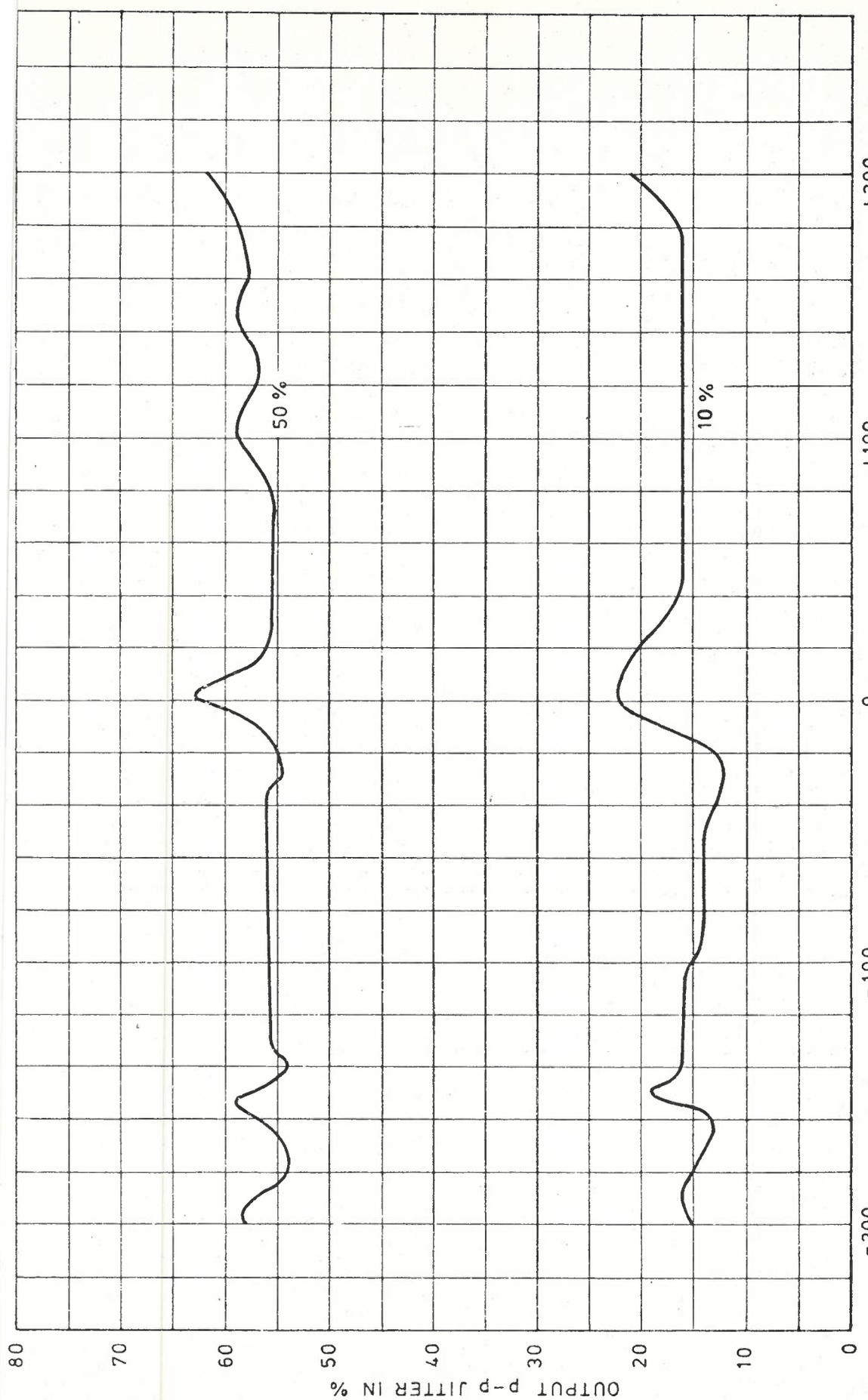


FIG. 10 MEASURED OUTPUT JITTER OF 8448 kbit/s SYSTEM WITH 10 % AND 50 % p-p 10 Hz SINEWAVE INPUT TRIBUTARY JITTER

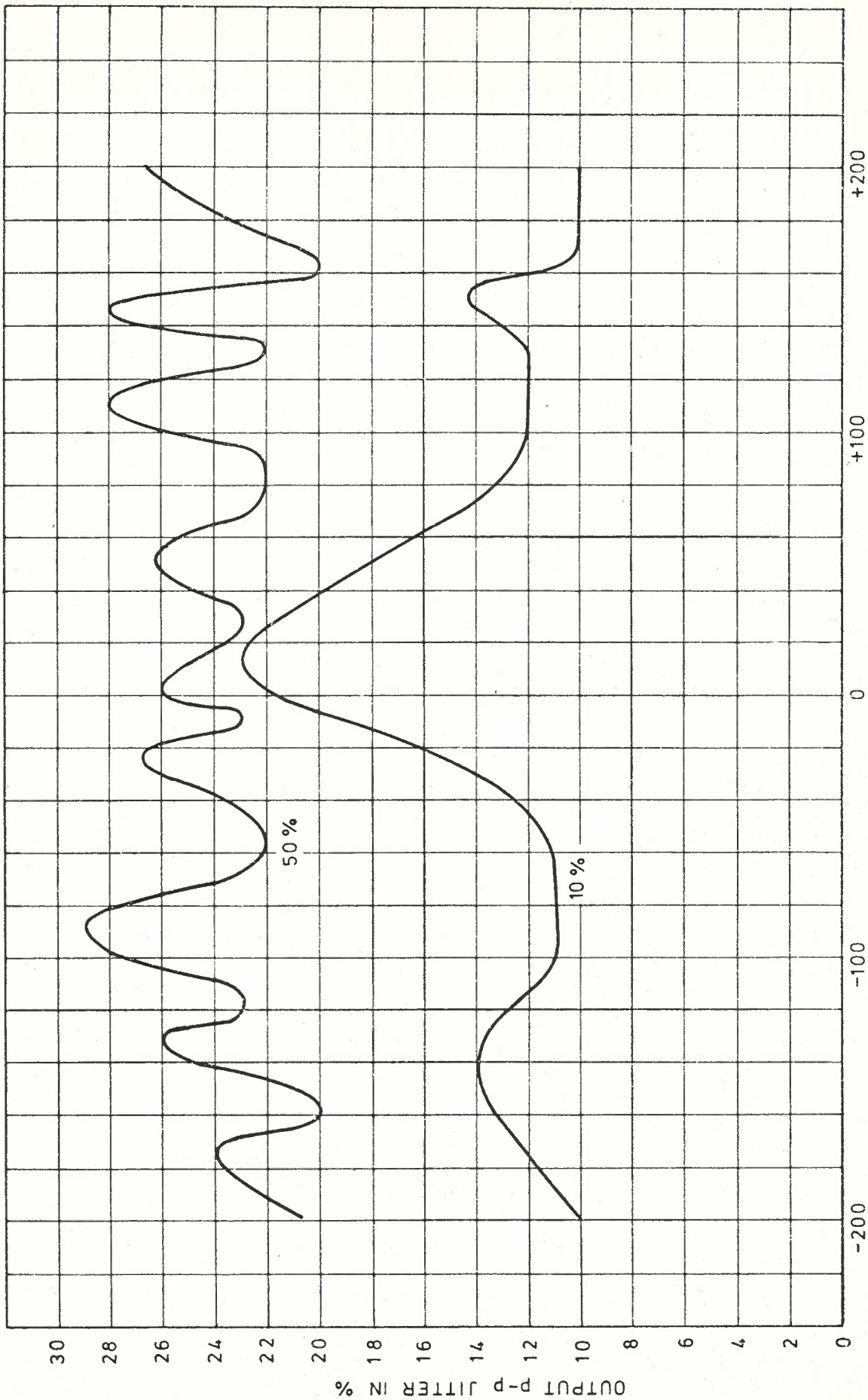


FIG. 11 MEASURED OUTPUT JITTER OF 6312 kbit/s SYSTEM WITH 10 % AND 50 % p-p 100 Hz SINEWAVE INPUT TRIBUTARY JITTER

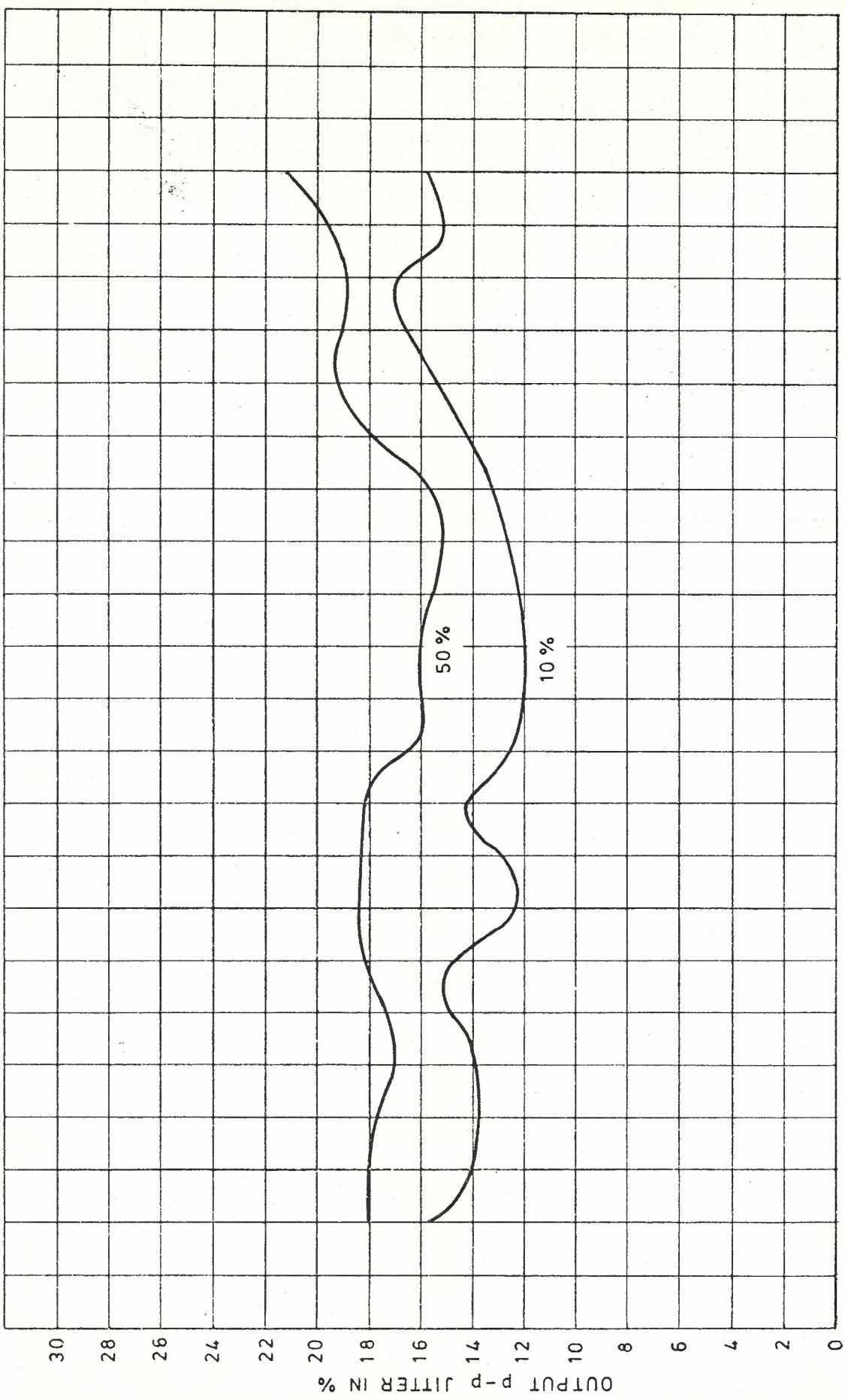


FIG. 12 MEASURED OUTPUT JITTER OF 8448 kbit/s SYSTEM WITH 10% AND 50% p-p 100 Hz SINEWAVE INPUT TRIBUTARY JITTER.

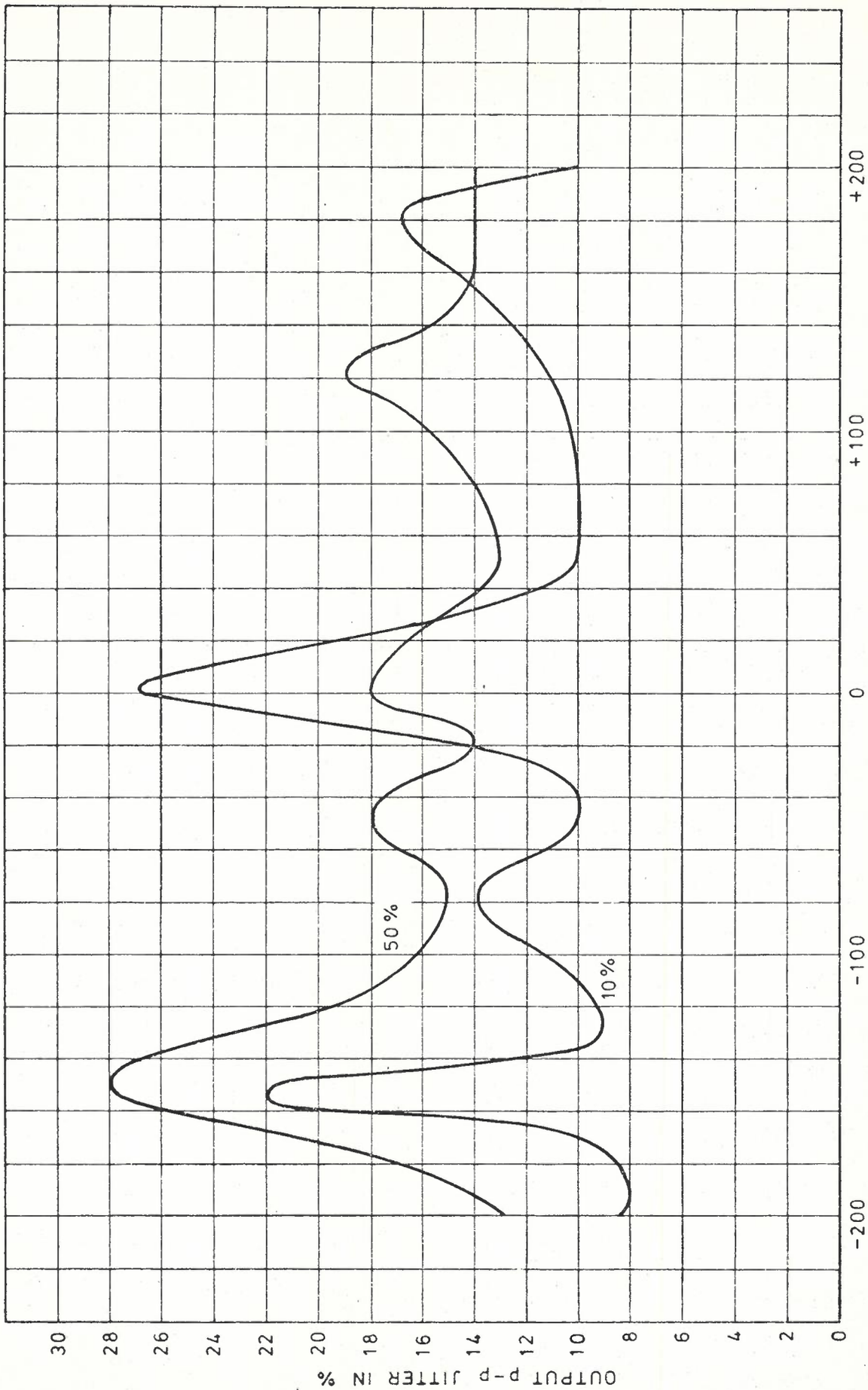


FIG. 13 MEASURED OUTPUT JITTER OF 6312 kbit/s SYSTEM WITH 10% AND 50% p-p 500 Hz SINEWAVE INPUT TRIBUTARY JITTER.

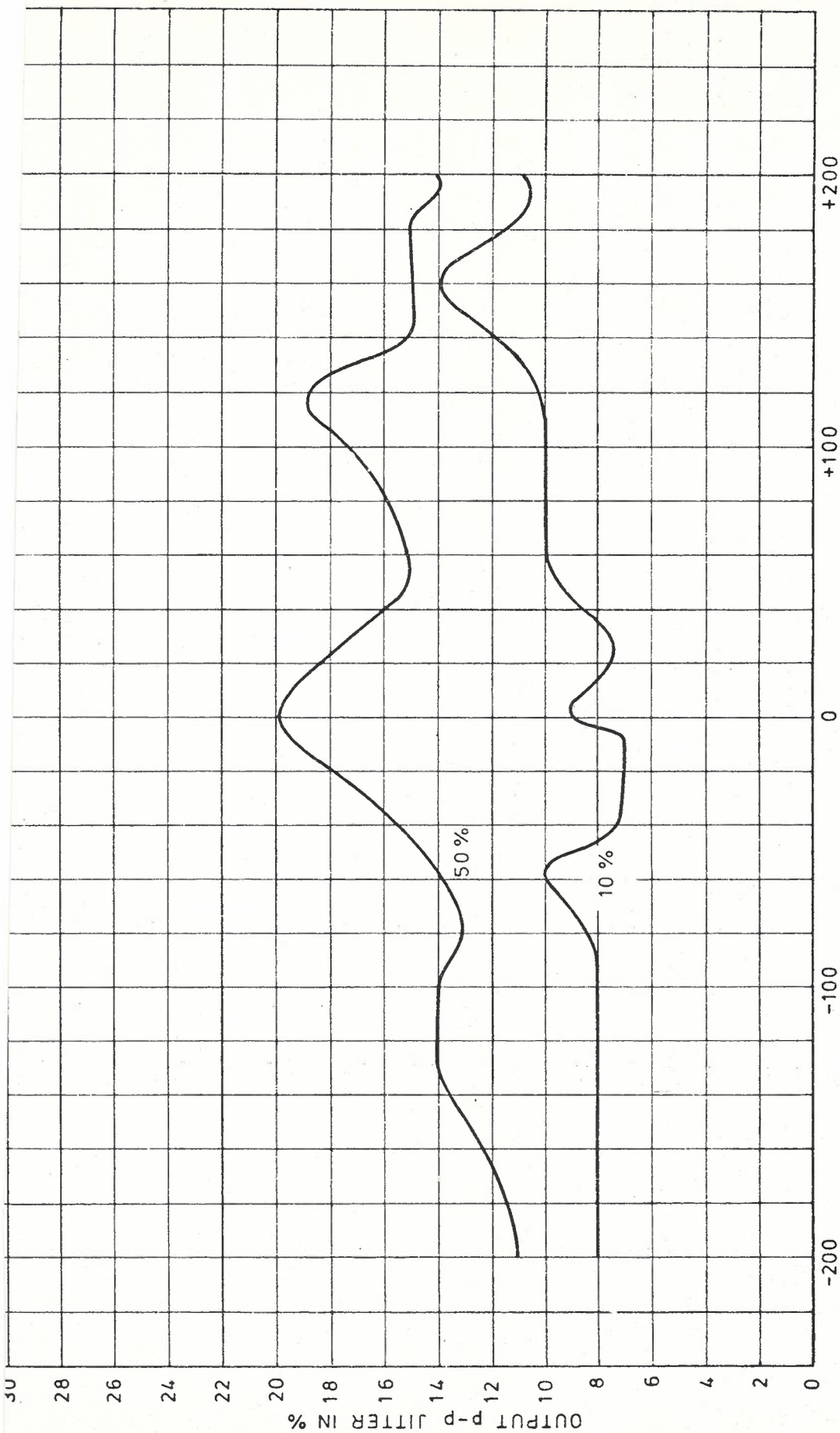


FIG. 14 MEASURED OUTPUT JITTER OF 8448 kbit/s SYSTEM WITH 10% AND 50% p-p 500 Hz SINEWAVE INPUT TRIBUTARY JITTER.

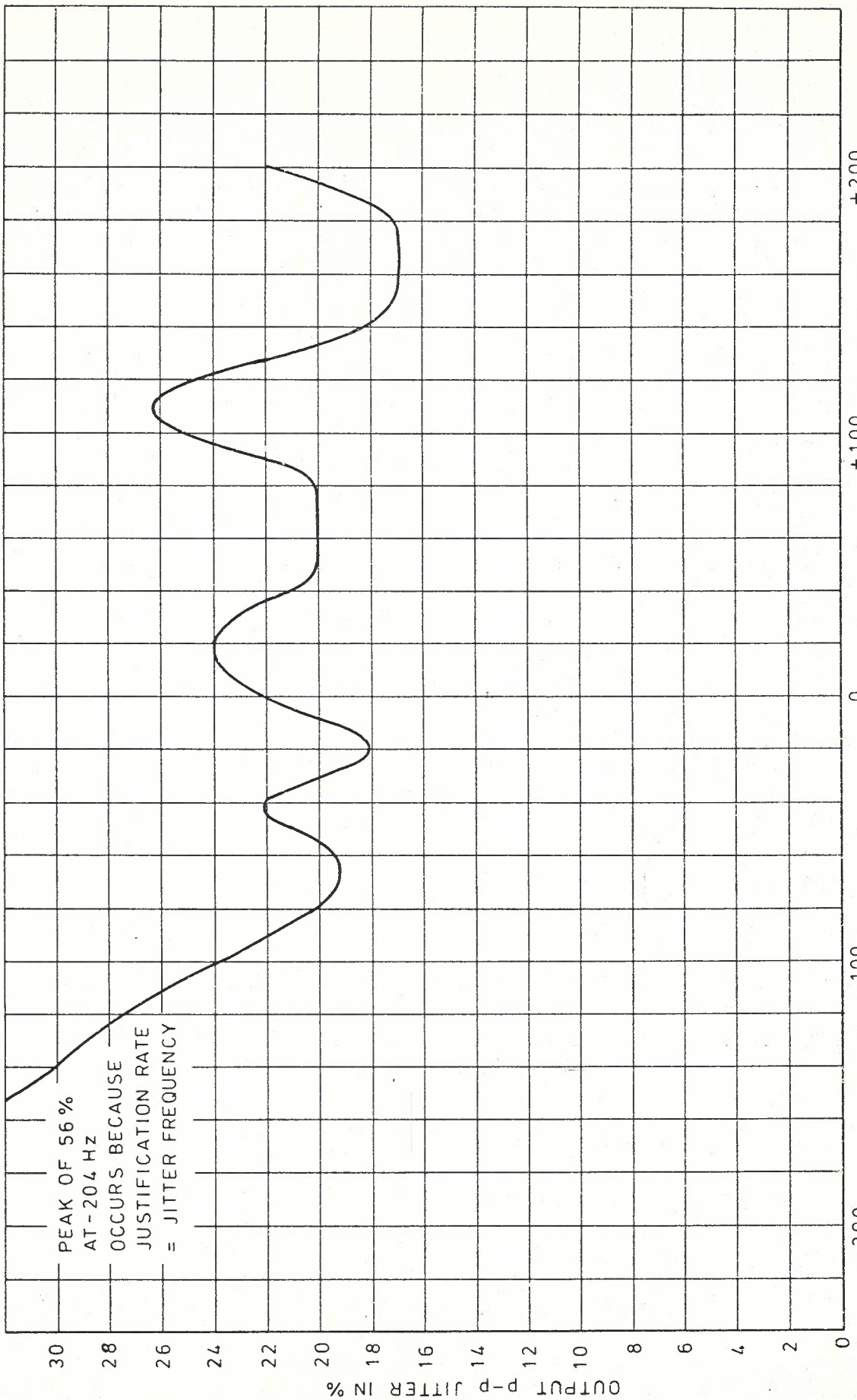


FIG. 15 MEASURED OUTPUT JITTER OF 6312 kbit/s SYSTEM WITH 50 % p-p 2kHz SINEWAVE INPUT TRIBUTARY JITTER.

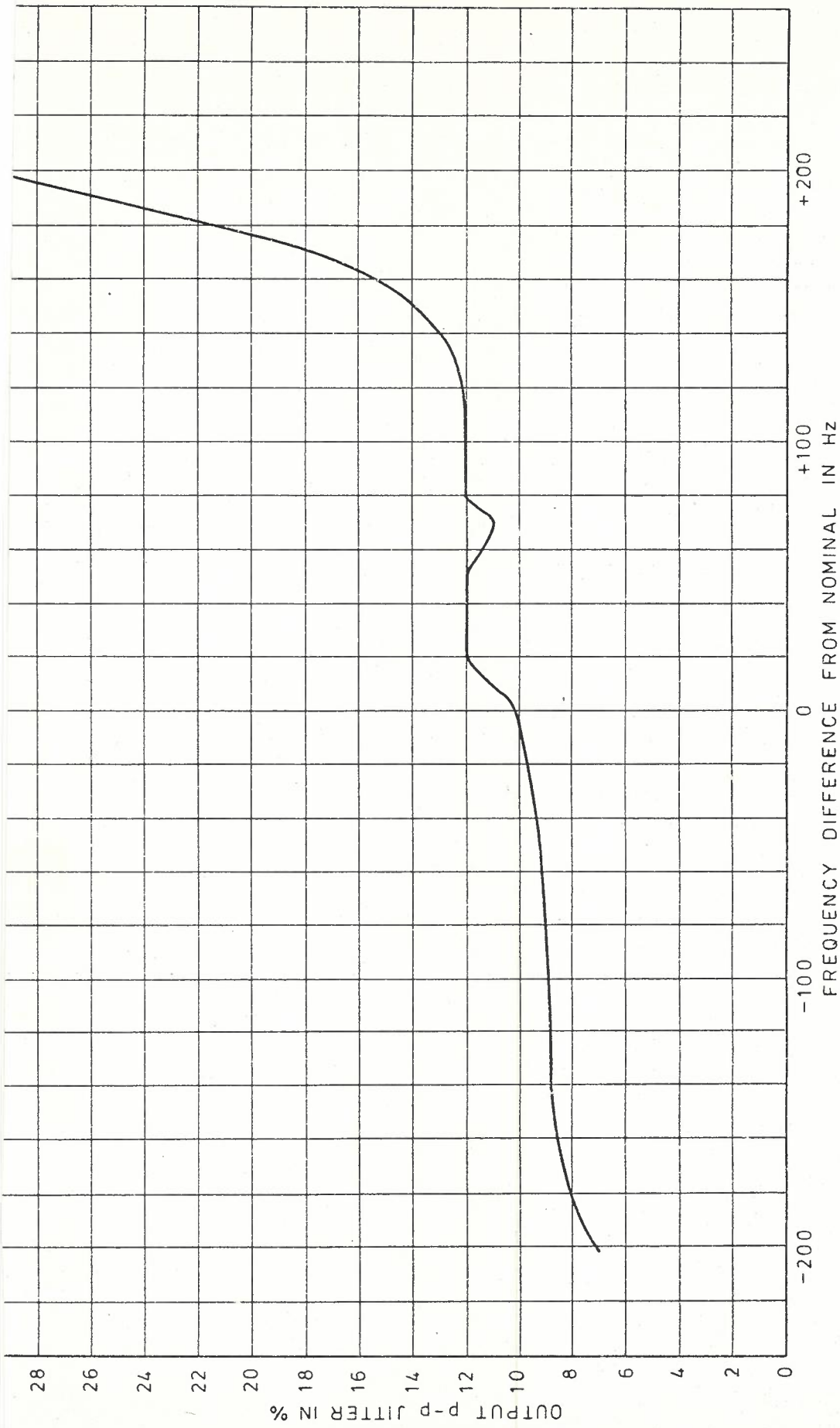


FIG. 16 MEASURED OUTPUT JITTER OF 8448 kbit/s SYSTEM WITH 50% p-p 2 kHz SINEWAVE INPUT TRIBUTARY JITTER.

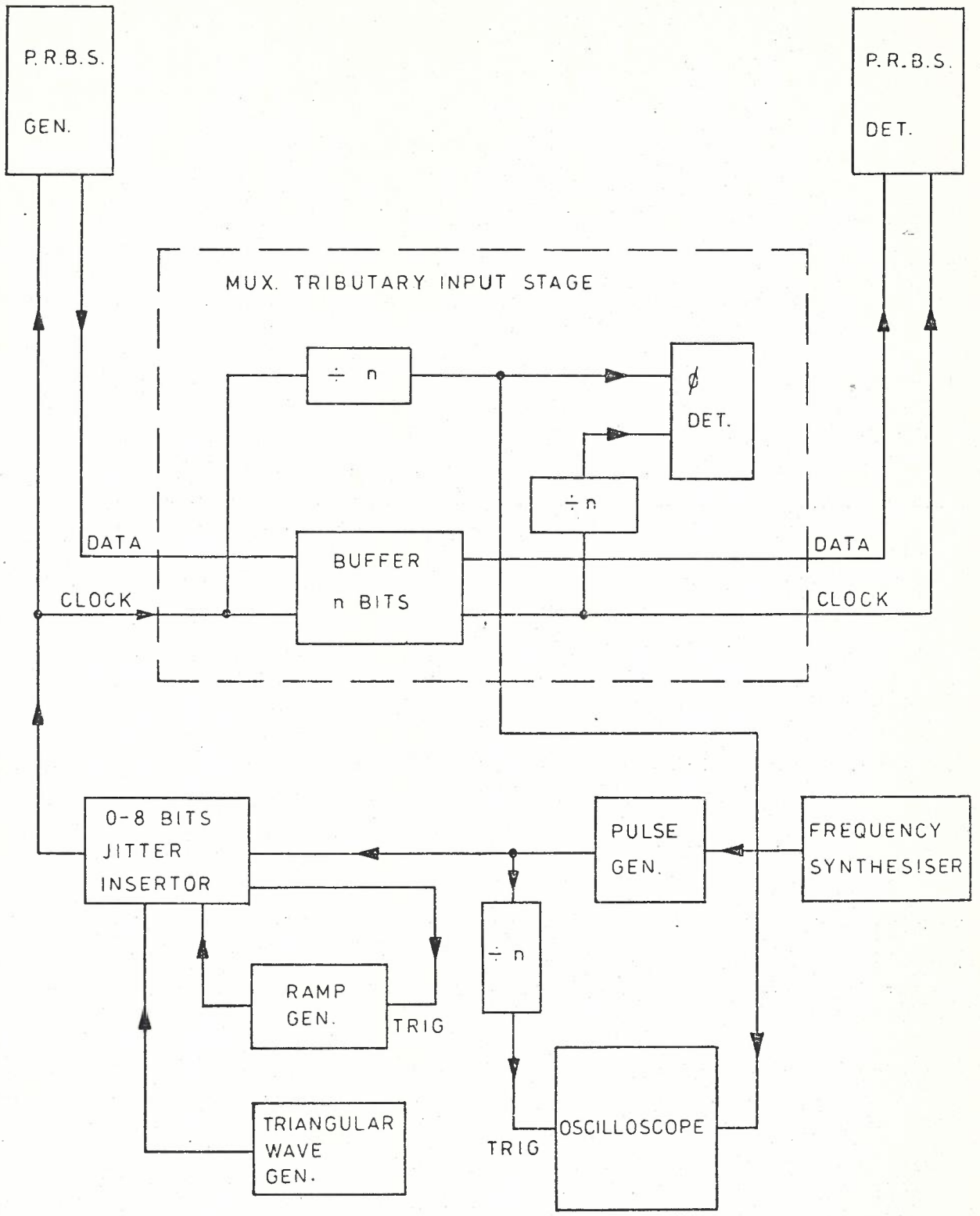


FIG. 17 TEST SETUP FOR MEASUREMENT OF JITTER TOLERANCE OF THE TRIBUTARY INPUT BUFFER.

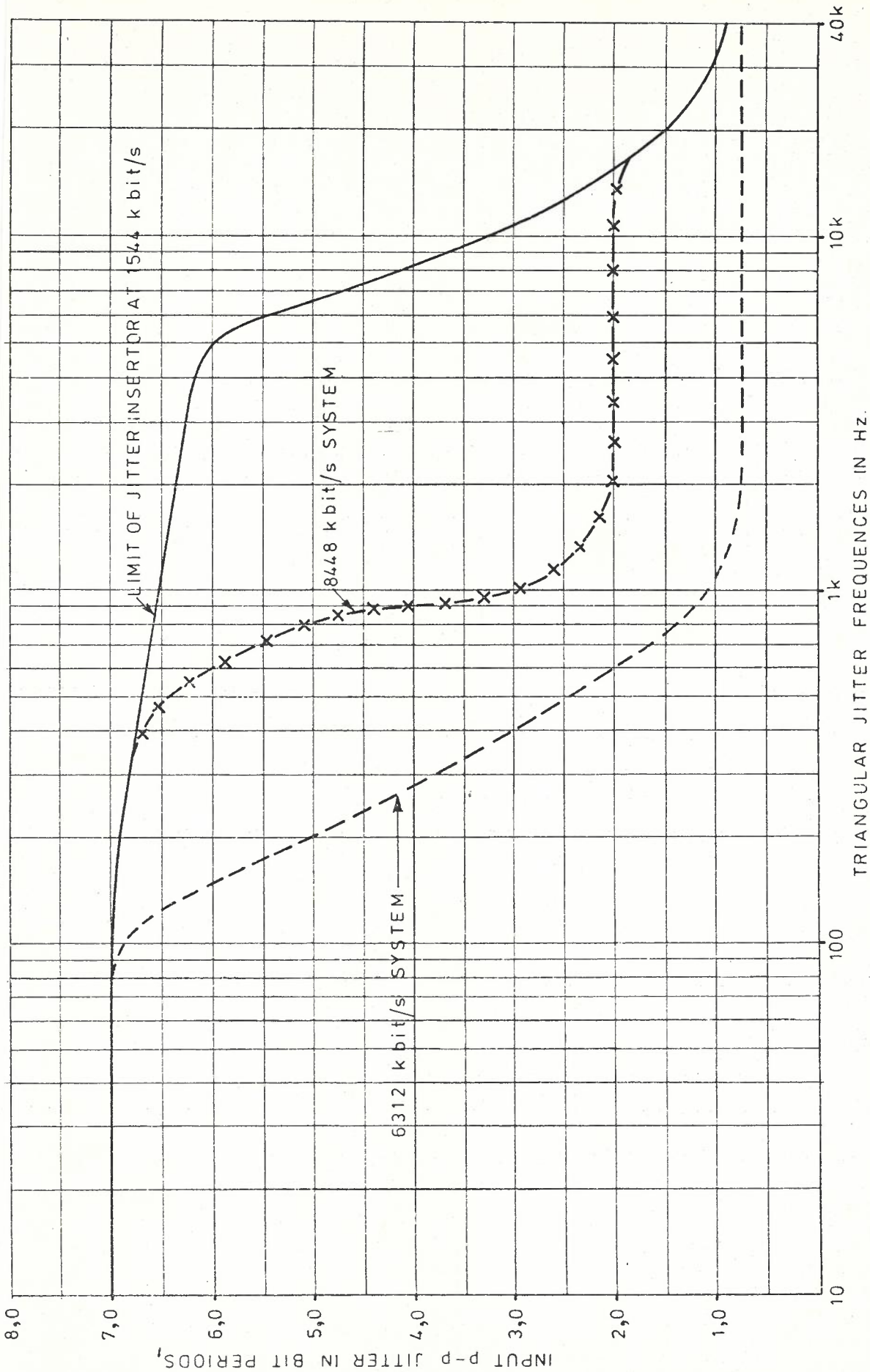


FIG. 18 MAXIMUM TRIANGULAR JITTER ALLOWABLE VS JITTER FREQUENCY FOR SIGNALS APPLIED TO THE TRIBUTARY INPUT OF THE 6312 k bit/s AND 8448 k bit/s SYSTEMS.

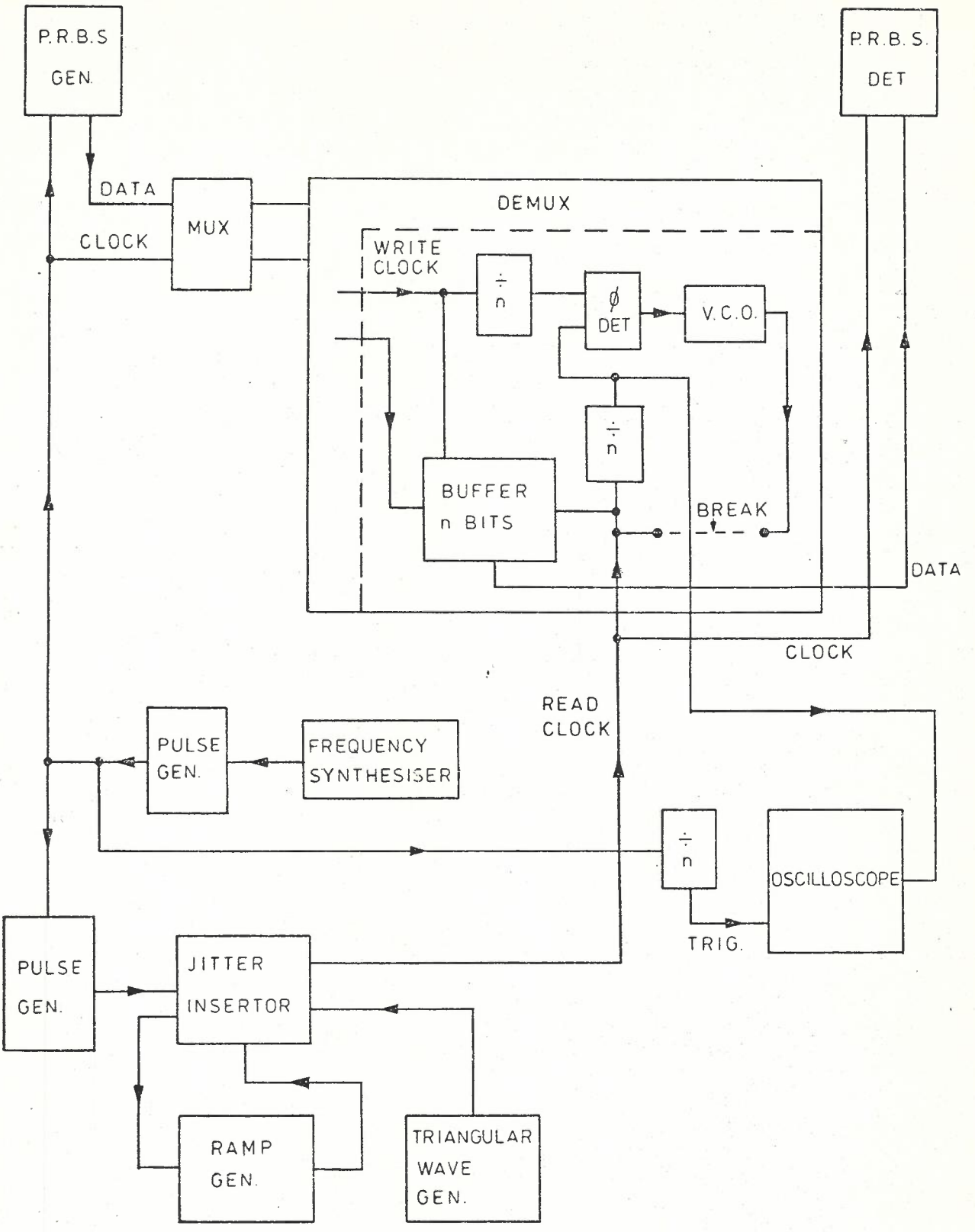
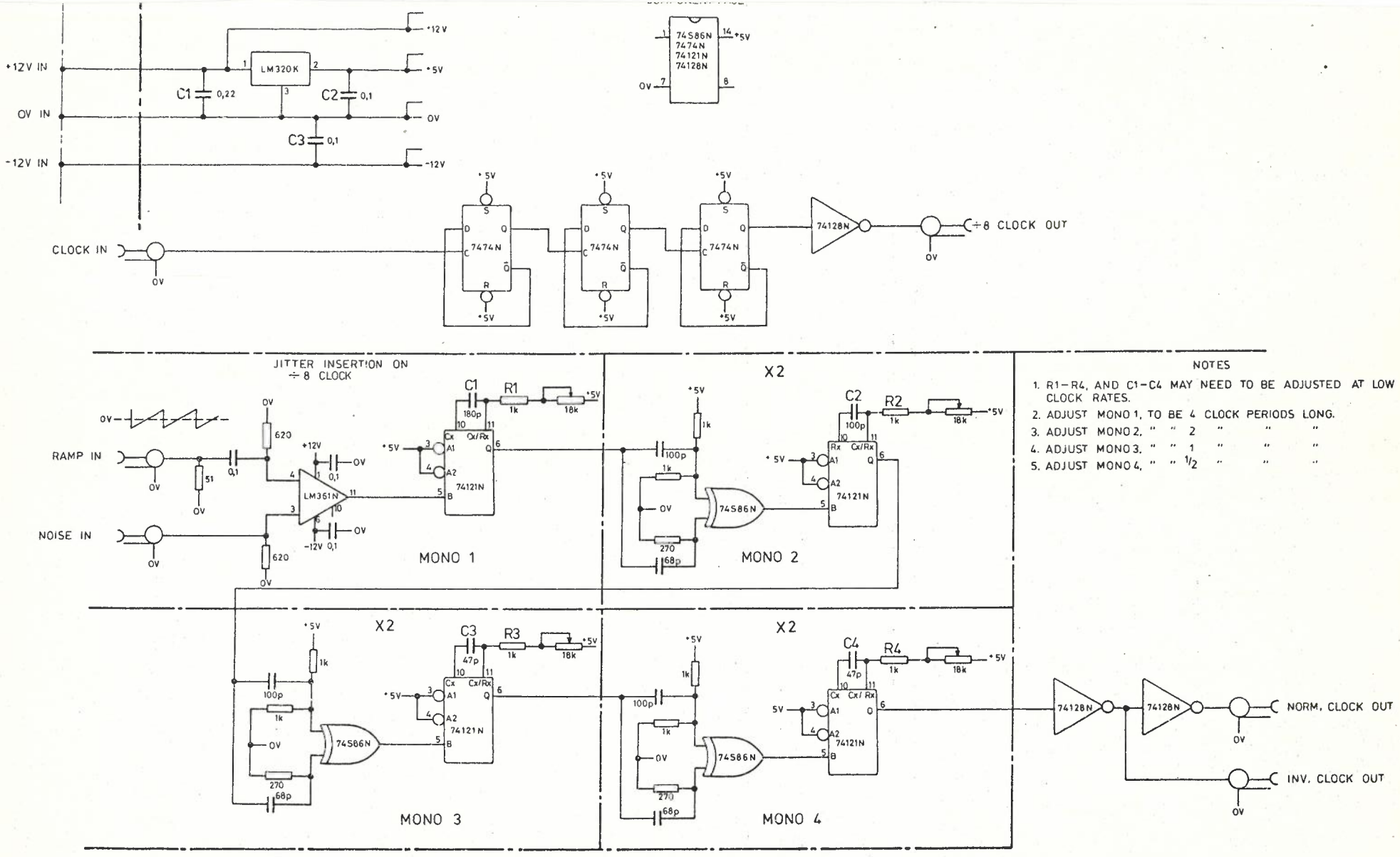


FIG. 19 TEST SETUP FOR MEASUREMENT OF RECEIVE BUFFER SPARE CAPACITY.



NOTES

1. R1–R4, AND C1–C4 MAY NEED TO BE ADJUSTED AT LOW CLOCK RATES.
2. ADJUST MONO 1, TO BE 4 CLOCK PERIODS LONG.
3. ADJUST MONO 2, " " 2 " " "
4. ADJUST MONO 3, " " 1 " " "
5. ADJUST MONO 4, " " $\frac{1}{2}$ " " "

CIRCUIT 1. 0-8 bit PERIOD JITTER INSERTOR