CP 310
PRICE 20c

THE AUSTRALIAN POST OFFICE

COURSE OF TECHNICAL INSTRUCTION

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D.C RESTORATION AND CLAMPING

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1. INTRODUCTION.

1.1 Many pulse circuits rely for their correct operation on the presence of a D.C. component in the signal. It is not always economical to preserve the D.C. component throughout the entire system, as design of direct coupled amplifiers is complicated when many stages are necessary. It is sometimes more convenient to amplify and transmit only the A.C. component of the signal, and then to reinsert the D.C. component at points where it is required. The term used to describe the action of reinserting the D.C. component and also low frequency components of a signal which have been lost or attenuated by a transmission system, is "D.C. restoration."

The importance of the D.C. component in a television signal and the advantages of D.C. amplification and D.C. restoration are discussed in the paper "Composite Video Signals". A number of places where the D.C. component is required in a television system are included in paragraphs 4.4 to 4.7 of this paper and when the D.C component is not maintained at these points by a D.C. transmission system, D.C. restoration is used.

1.2 Since the D.C. component of a television signal varies with the picture information, the reinsertion of the D.C. component cannot be achieved by adding a fixed voltage to the signal. This is also the case for other signals where D.C. restoration is required.

The restoration of the D.C. component depends on the fact that a particular section of the waveform, often the positive or the negative peak, should be at a certain level. The reinsertion of the correct D.C. component is accomplished by circuits which arrange to "clamp" the required section of the waveform at the desired reference voltage. D.C. restoration is possible with television video signals because specific levels, namely the blanking level and the synchronizing pulse level, repeat at regular intervals. By "clamping", the D.C. component is restored and, in addition, low frequency distortion and interference is reduced.

1.3 This paper examines circuits that can be used to achieve D.C. restoration by clamping, and practical disadvantages of the circuits are discussed. As many of the circuits find their main applications in television installations, examination of their operation is often with composite video signal inputs.

2. PEAK RECTIFIER CLAMP CIRCUITS.

2.1 Coupling Circuit followed by Shunt Diode. When a signal containing a D.C. component is passed through a resistor-capacitor coupling circuit, the D.C. component is removed and only the A.C. component appears across the output. Consider now what happens to the waveform when a diode is shunted across the output as in Fig. 1a. When the anode of the diode is positive with respect to its cathode, the diode conducts and represents a relatively low value of resistance. The equivalent circuit for this condition is as in Fig. 1b. When the diode anode is negative with respect to its cathode, the diode is non-conducting and therefore represents an open circuit. The equivalent circuit in this case is that of a coupling circuit. (Fig. 1c).

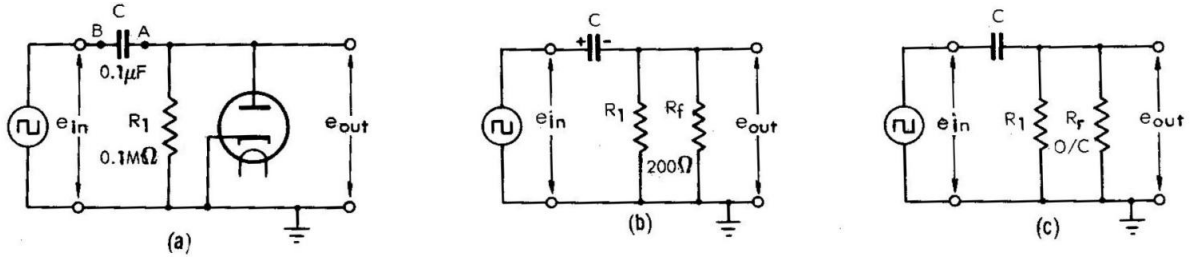


FIG. 1. POSITIVE PEAK RECTIFIER CLAMP.

The resistance represented by the diode in its conducting and non-conducting directions depends on the type of diode considered. As the characteristic of voltage versus current for a diode is non-linear, the resistance of the conducting diode depends on the section of the characteristic in use. Typical values of forward resistance for small high-vacuum diodes are 500Ω to 200Ω and for germanium or silicon diodes are 200Ω to 50Ω as the current increases from about 1mA to 10mA. However, at lower currents (approximately 100μA) semi-conductor diode forward (conducting) resistance rises to several thousand ohms. The high-vacuum diode characteristic is also complicated in the region of the changeover from conduction to non-conduction by contact potential, which depends on the differences in temperatures and material composition of the electrodes, and also by the initial velocity of the electrons emitted from the cathode. Because of these facts the anode of a high vacuum diode must be slightly negative before abode current ceases.

The reverse resistance of high-vacuum and silicon diodes is practically infinite, but germanium diodes normally have a resistance of approximately 1MΩ at room temperature, decreasing to the order of 0.1MΩ at their maximum operating temperature. These values of reverse (non-conducting) resistance must, therefore, be taken into account when assigning practical values to the equivalent circuits in Figs.1b and c. In our examination of clamp circuits using diodes, we will consider an ideal diode in which the resistance in the non-conducting direction is infinite, and the resistance in the conducting direction (R_f) is constant at 200Ω, giving a forward characteristic that is linear.

2.2 The 500c/s 100V peak-to-peak square wave of Fig. 2a is applied to the circuit in Fig. 1a. On the application of the first positive half cycle, with no initial charge on the capacitor, the full +50V appears at the output. The diode under these conditions is conducting and the capacitor is charged quickly to 50V (with a polarity as shown in Fig. 1b) through the low value of resistance of the diode. The shunt resistance in parallel with the conducting diode is high by comparison with the diode resistance of 200Ω and can be neglected. The time constant of the charge circuit is:-

$$\tau_c = CR_f$$

$$= \frac{0.1 \times 200 \times 10^6}{10^6} = 20\mu S.$$

Therefore the capacitor is fully charged in 100μS and the output voltage falls to zero at this time, remaining there for the rest of the positive half cycle.

At the commencement of the negative half cycle, e_{out} steps by 100V to -100V. The diode is now non-conducting and the discharge time constant of the capacitor circuit is:-

$$\tau_c = CR_1$$

$$= \frac{0.1 \times 10^6 \times 10^3}{10^6} = 10mS.$$

The duration of the negative half cycle of the square wave therefore represents 0.1 time constants and in this time the output voltage falls from -100V to 90.48V (approximately 90V) and the capacitor voltage falls from 50V to approximately 40V. With the next positive half cycle the output makes appositive step to approximately +10V and again the diode is conducting and the capacitor is quickly recharged to 50V. This process then repeats itself every cycle giving an output voltage as shown in Fig. 2b.

Notice that the output waveform has its positive peak established at the zero axis except for the small time that the capacitor is charging. That is, except for an overshoot, the extreme of the waveform is fixed at the potential at which the diode commences to conduct. The output waveform is now practically all negative and a negative D.C. component is present. The D.C. component is developed by rectification of the peaks of the input signal and its magnitude is equal to the magnitude of the capacitor voltage illustrated in Fig. 2c. An increase of the discharge time constant of the circuit reduces the variation of e_c and the tilt and overshoot on the output waveform.

The circuit still clamps the positive peak of the waveform at the zero axis when a D.C. component is present at the input. The only change is in the magnitude of the capacitor voltage.

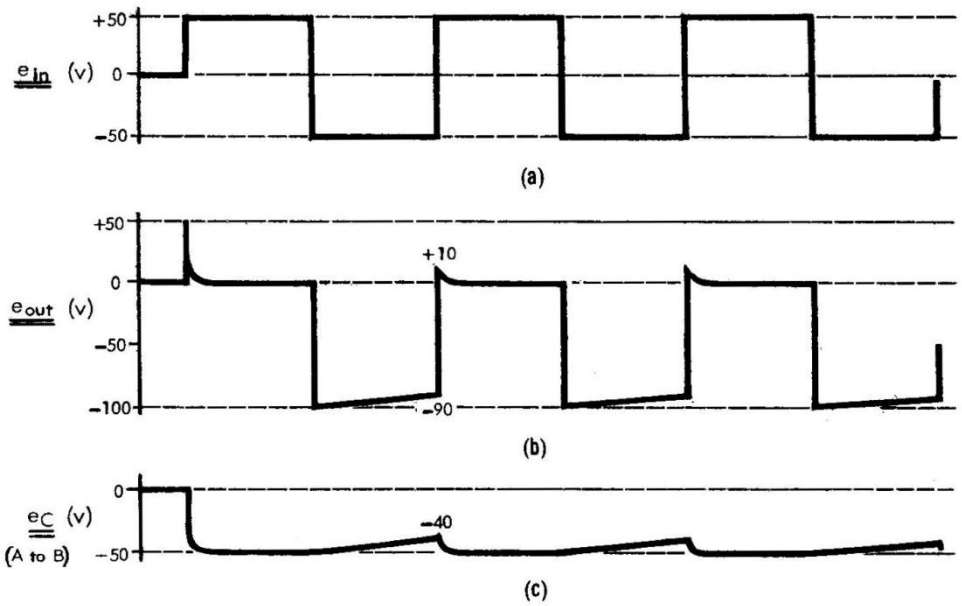


FIG. 2. POSITIVE PEAK RECTIFIER CLAMP WAVEFORM.

Suitable titles for the circuit in Fig. 1a are, peak rectifier clamp, peak rectifier D.C. restorer or simply D.C. restorer. The latter general title is commonly used, but because this title fits a number of circuits, it does not describe this particular circuit very well. Since the circuit clamps the positive extreme of the waveform, and, in doing so, introduces a negative D.C. component, it is a positive peak rectifier clamp or a negative D.C. restorer. The latter title can be confusing when considering titles for biased circuits.

2.3 Negative Peak Rectifier Clamp. If the connections to the diode in the circuit of Fig. 1a are reversed and the circuit is as shown in Fog. 3a, the output waveform produced has its negative extreme clamped at a fixed voltage and a positive D.C. component is introduced. The output waveform is as in Fig. 3c. This circuit is a negative peak rectifier clamp, or a positive D.C. restorer.

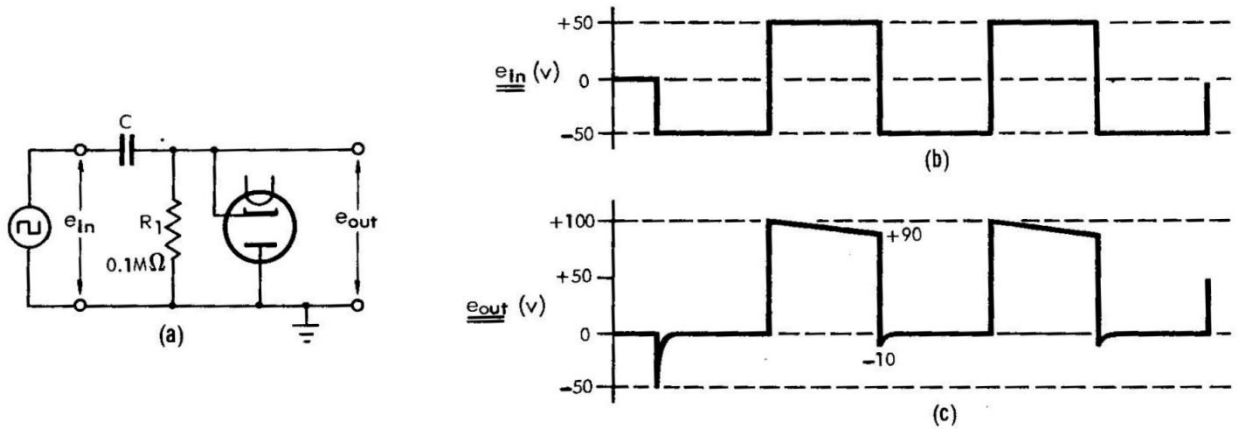


FIG. 3. NEGATIVE PEAK RECTIFIER CLAMP.

A convenient way of estimating the position of the output waveform is to consider that the input waveform attempts to shift so that the diode never conducts. In Fig. 3a the diode would conduct if the output became negative with respect to earth, so the output waveform shifts until (except for the overshoot which charges the capacitor) its extreme does not extend into the negative region.

2.4 Biassed Clamp Circuits. The peak rectifier clamp can be arranged to clamp the extreme of the waveform at potentials other than zero by adding a bias voltage in the return circuit of both the diode and the resistor as in Fig. 4a. With the polarities and values as shown, the circuit is a positive peak rectifier clamp with a negative bias of 40V. Since the peak rectifier clamp establishes the extreme of the waveform at the potential which causes the diode to conduct, the output waveform from this circuit has its positive extreme clamped at -40V. The bias voltage is the reference potential to which the extreme of the waveform is clamped.

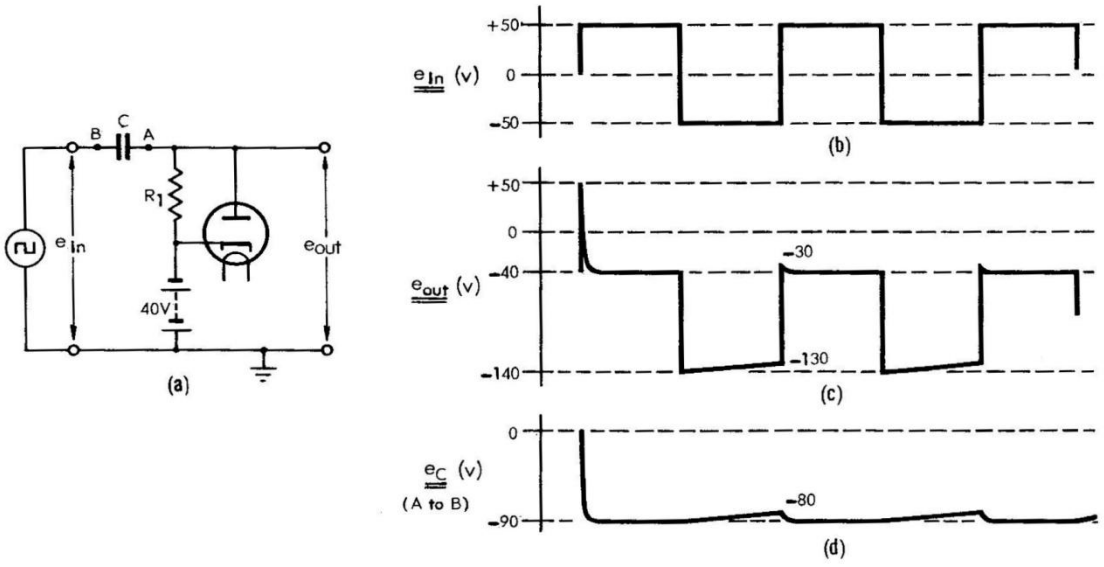


FIG. 4. POSITIVE PEAK RECTIFIER CLAMP WITH NEGATIVE BIAS.

Except for the initial charging of the capacitor, the only difference in the operation of the circuit containing a bias voltage from the circuit with no bias, is the operation of the potential to which the waveform is clamped. Examination of the operation in more detail illustrates this point. Consider in Fig. 4a that initially the capacitor is uncharged and that the 500c/s 100V p-p square wave is connected at the instant on a positive transition when the amplitude is zero as shown in Fig. 4b. The +50V applied to the input is immediately present at the output (Fig. 4c) and this and the -40V bias produces 90V across the diode in the conducting direction. The capacitor voltage (Fig. 4d) changes exponentially in a short time (100µS) to the -90V (point A relative to point B) of the input voltage and the bias voltage in series and at the same time the output voltage changes exponentially to equal the bias voltage of -40V.

At the commencement of the next half cycle the input steps by 100V in the negative direction to -50V. The output voltage also steps -100V to -150V and therefore the diode is non-conducting. During the negative half cycle of the input square wave the capacitor discharges via the resistor (R_1), the circuit time constant being 10mS, and the output voltage changes from -140V towards the bias voltage. At the end of the half cycle, the output voltage has changed by approximately 0.1 (0.0952) of the 100V acting in the discharge circuit, that is by 10V to -130V. At the same time the capacitor voltage changes by 10V from -90V to -80V.

With the next positive half cycle, the output voltage steps in a positive direction by 100V to -30V. With -30V on its anode and -40V on its cathode the diode conducts, and e_{out} returns to the bias voltage of -40V as the capacitor is recharged to 90V.

The output waveform in Fig. 4c shows that, except for the overshoot produced during the charging of the capacitor, the positive extreme of the output is clamped to -40V.

When the polarity of the bias is reversed as in Fig. 5a, the positive extreme of the output waveform is clamped to +40V. Consider again that the capacitor has no initial charge and that the input square wave is applied at zero on a positive transition as shown in Fig. 5b. The output voltage (Fig. 5c) steps instantly to +50V and this makes the diode anode 10V positive with respect to its cathode causing it to conduct. The capacitor is charged in a short time constant circuit to the input voltage and the bias voltage in series so that the voltage across it (Fig. 5d) is -10V (point A relative to point B). With this charging of the capacitor the output voltage quickly varies exponentially to equal the bias voltage of +40V.

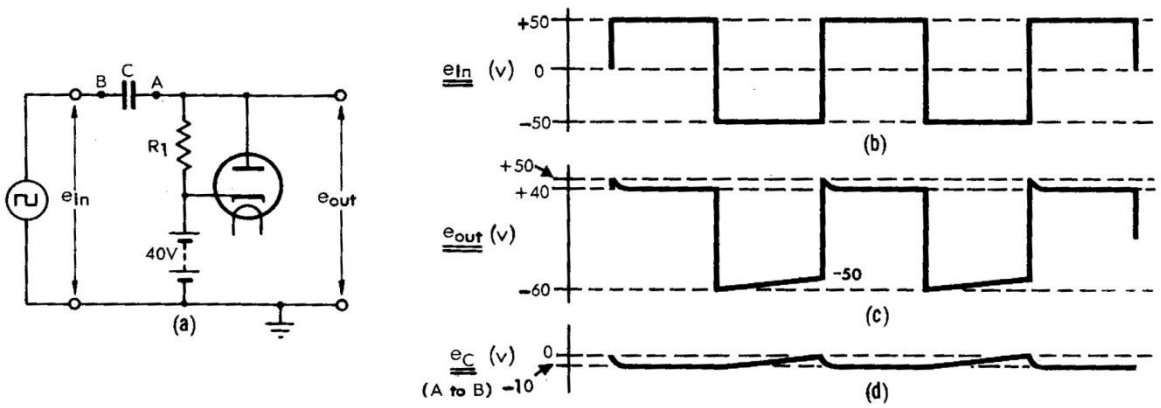


FIG. 5. POSITIVE PEAK RECTIFIER CLAMP WITH POSITIVE BIAS.

At the commencement of the negative half cycle, the output steps in the negative direction by 100V to -60V and the diode becomes non-conducting. During the negative half cycle, the output voltage changes towards the bias voltage of +40V and in the 0.1 time constants of the half cycle, changes by 10V to -50V. With the next positive half cycle the output steps to +50V but quickly returns to +40V after the recharging of the capacitor to -10V through the conducting diode. Notice that, except for the initial charging of the capacitor, the output wave shape is identical with the examples with no bias and with a negative bias voltage.

If in the circuit of Fig. 5, the bias voltage exceeds the peak input voltage, the clamping action cannot commence immediately. Consider, for convenience, that the input signal is a 200c/s square wave with an amplitude of 20V p-p, and the bias voltage is still +40V. The output waveform for this condition is shown in Fig. 6. Initially the voltages are such that the diode is maintained non-conducting, and the circuit is equivalent to a coupling circuit. The output voltage gradually drifts, attempting to become symmetrically positioned about an axis set by the bias voltage. However, after a number of cycles, when the positive peak of the output waveform has reached +40V, the clamp action commences as shown in Fig. 6b. In less than five times the time constant (CR_1) the output waveform is exactly as the final waveform in Fig 5c.

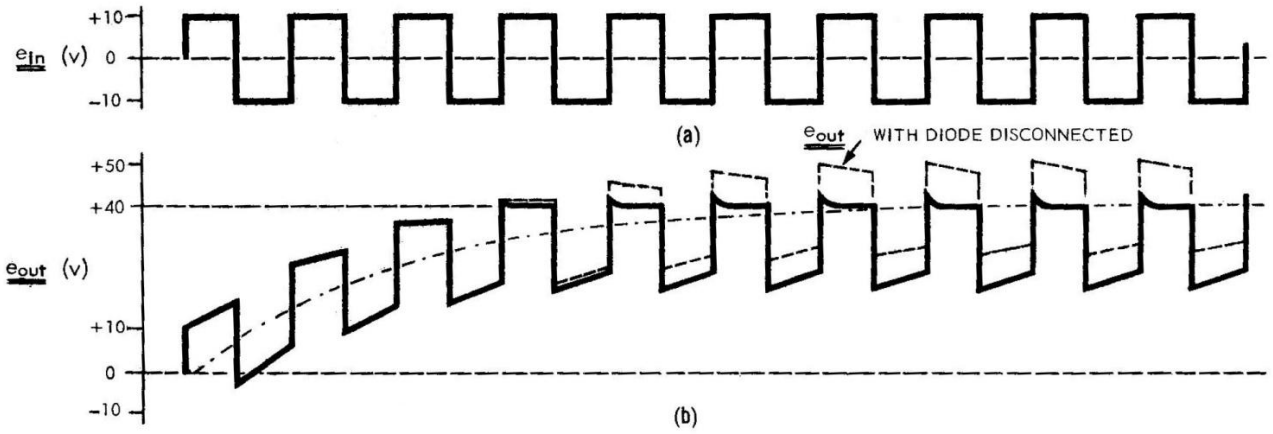


FIG. 6. POSITIVE PEAK RECTIFIER CLAMP WAVEFORMS.

Bias can be applied to negative peak rectifier clamp as is shown in Fig. 7. In Fig. 7a, the negative extreme of the waveform is clamped to +40V and in Fig. 7b the negative extreme of the waveform is clamped to -40V. With Fig. 7b, when the signal has an amplitude smaller than the bias voltage, a delay is likely to occur in the clamping action while the capacitor charge establishes its correct value via the high value of shunt resistance.

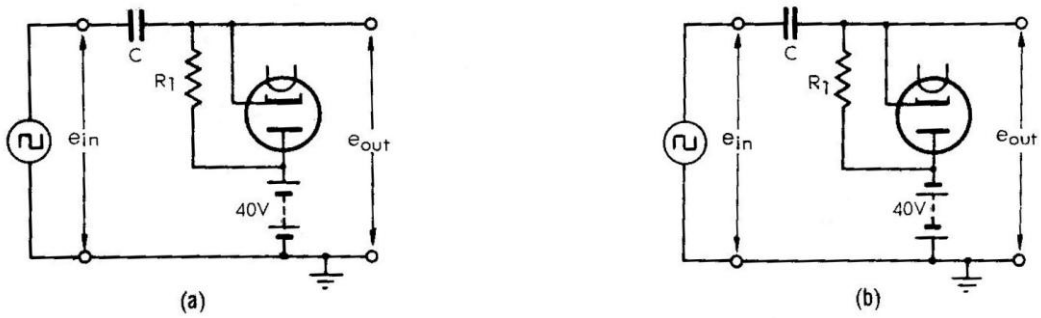


FIG. 6. NEGATIVE PEAK RECTIFIER CLAMPS WITH BIAS.

2.5 Effect of Source Resistance. In paras. 2.1 - 2.4, high voltages appear directly across the diodes of the circuits. These voltages could only occur with practical diodes in the presence of extremely high diode currents that would be sufficient to ruin the diode. In practical circuits, overloading of the diode by exceeding its maximum current rating must be avoided, but because of the source resistance, excess currents do not often occur.

Consider a positive peak rectifier clamp fed from a typical value of source resistance of 1,800Ω (Fig. 8a). This resistance is included in both the charge and the discharge circuits of the capacitor. It is small enough by comparison with the shunt resistor R_1 to be neglected when the diode is non-conducting, but it multiplies by 10 the charge time constant of the capacitor circuit when the diode is conducting.

The charge time constant of the capacitor circuit is:-

$$\tau_C = C(R_f + R_S)$$

$$= \frac{0.1\ (200 + 1800)\ x\ 10^6}{10^6}$$

$$= 200\mu S$$

This means that, for the 500c/s input, it takes the complete half cycle of the signal for the output to change to the desired clamp voltage and for the capacitor to be given its correct charge.

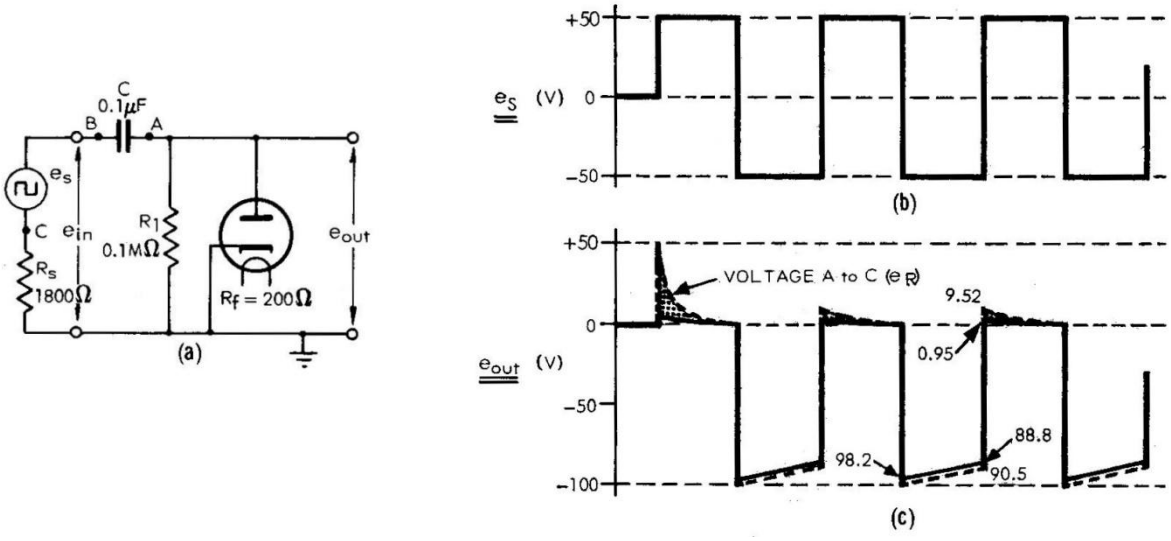


FIG. 8. CLAMP CIRCUIT WITH SOURCE RESITANCE.

In Fig. 8a, with a source voltage of 500c/s and 100V p-p, (as shown in Fig. 8b), and with no initial charge on the capacitor, the output voltage is as shown in Fig. 8c. The initial positive step of 50V causes the diode to conduct, and the voltage (e_R) across the total resistance of the circuit between A and C steps top +50V. However, only one tenth of this voltage step appears across the conducting resistance of the diode and, therefore, at the output. The voltage across the total resistance, and therefore the output voltage, decreases to zero in one half cycle of the input signal.

With the commencement of the negative half cycle a negative step of 100V occurs, and appears across the total circuit resistance. The diode becomes non-conducting, and, since R_1 is much greater than R_S, only a small voltage (approximately 1.8V) appears across the source resistance, with the major amount (approximately 98.2V) being at the output. During the negative half cycle the total resistor voltage decreases towards zero. The half cycle has a duration approximately equal to 0.1 time constants, and during this time the total voltage changes to 90.48V, and the output voltage to approximately 88.8V.

On the next positive step the total resistor voltage steps by 100V to +9.52V but the output rises to only +0.952V and then decreases exponentially to zero. The shaded area in Fig. 8c represents the section of the waveform lost in the source resistance. This section of the input is clipped off and does not appear at the output.

Notice that when the diode forward resistance is much smaller than the source resistance, the output voltage is clamped closer to the reference voltage. If the resistance of the conducting diode is zero, the output is clamped exactly to the reference voltage. However, the source resistance must also be low to prevent clipping of the clamped section of the waveform.

2.6 Effect of Pulse Duration. In many practical applications pulses with small pulse duty factors must be clamped to the reference potential. This often means that the short duration of the pulse does not allow the capacitor in the peak rectifier clamp to completely charge during the pulse duration. Consider that the pulse duty factor of the waveform in the previous examples is altered so that the input wave is now a rectangular wave with a pulse duty factor of 0.1 and a repetition frequency of 500c/s (pulse spacing of 2mS) as shown in Fig. 9a. This waveform is applied to the positive peak rectifier clamp from a generator with a source resistance of 1,800Ω as in Fig. 8a. The output voltage and the voltage across the total resistance of the circuit is shown in Fig. 9b.

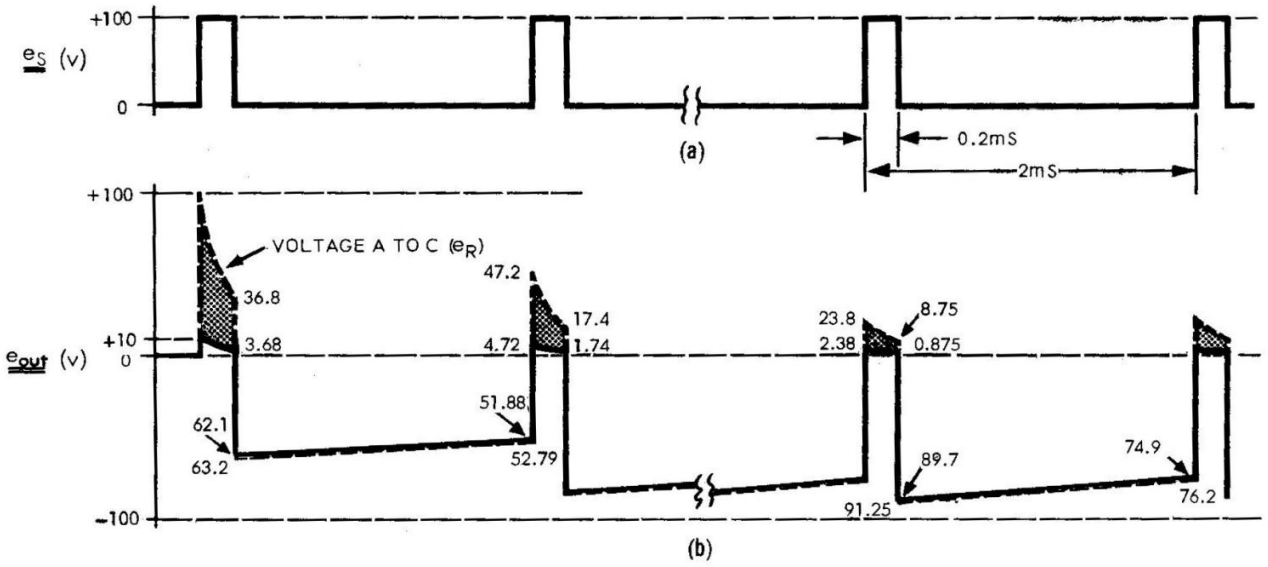


FIG. 9. SHORT DURATION PULSES.

With the application of the first pulse, the voltage across the total resistance of the circuit steps to +100V, but the output steps to only +10V. The diode is conducting so that the circuit time constant is 200µS. This is also the duration of the pulse, so during the time for the pulse the output falls to +3.68V.

With the negative step of 100V at the input the voltage across the total resistance steps by 100V to -63.2V and the output to -62.1V. During the next 1.8mS the total resistor voltage and the output voltage decrease exponentially towards zero and become -52.79V and -51.88V respectively. At the commencement of the next pulse the total resistor voltage steps to +47.2V and the decreases during the pulse duration equal to one time constant, to +17.4V. The output voltages at these times are a tenth of these voltages and are +4.72V and +1.74V respectively.

After a number of cycles the output voltage gradually shifts so that the positive peak becomes closer to the clamp potential, but actually never reaches it. The repetitive waveform varies from +2.38V at the commencement of the pulse to +0.875V at the conclusion, then steps to -89.7V and decreases exponentially to -74.9V between pulses.

The output waveform deviates further from the correct clamping potential in this example than it does for a square wave input (Fig. 8). It is much harder to achieve correct clamping to the pulse peak when the pulse duty factor is reduced.

The error would have been much greater except that the source resistance is much greater than the diode resistance. This has reduced the error, but has produced a large reduction in level, the significant reduction being produced during the clamping time. The clamped extreme of the waveform is clipped during the time that the diode is conducting because of the loss in the source resistance. Even more important than the overall amplitude change, is the change in relative levels that would be produced on a more complicated signal, such as a composite video signal in a television system.

2.7 As a simple way of obtaining an approximate idea of the clamping level when complicated waveforms are considered, the area of the waveform above and below the clamping reference voltage is investigated. In a coupling circuit where both the charge and the discharge circuits are identical, the output waveform establishes its position vertically so that the area of the waveform above the axis equals the area below the axis. In the peak rectifier clamp the time constant of the capacitor charge circuit through the diode is much shorter than that of the discharge circuit when the diode is non-conducting. For this circuit, the output waveform establishes itself so that the ratio of the two areas is in the same ratio as the time constants of the circuit under the two conditions. In Fig. 8a, the charge time constant is 200µS, the discharge time constant is 10mS, and the diode conducts when the output is positive. Therefore the ratio of the positive area to the negative area of the output waveform equals the ratio of 200µS to 10mS = 0.02.

As the conducting time of the diode is only one ninth of the non-conducting time, the average amplitude of the positive section of the wave is 9 x 0.02 = 0.18 times the average amplitude of the negative section.

$$\therefore \text{The average positive amplitude} = \frac{0.18}{1.18} \times 100$$

$$= 15.26V.$$

$$\therefore \text{The average negative amplitude} = \frac{1}{1.18} \times 100$$

$$= 84.74V.$$

Notice that the average values as illustrated in Fig. 10. Agree closely with the average of the values of the total resistor waveform in Fig. 9. Exact agreement is approached when both the charge and the discharge times of the capacitor are short compared with the respective circuit time constants. This occurs when the capacitor is large enough so that negligible change of charge occurs during the discharge time, and therefore also during the charge time.

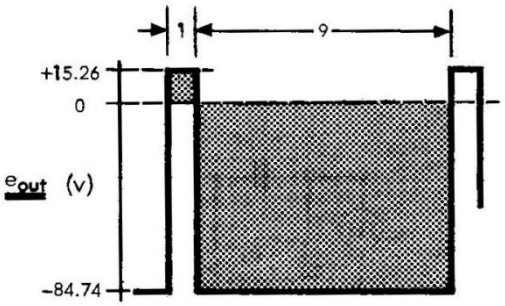


FIG. 10. AVERAGE VALUES OF TOTAL RESISTOR VOLTAGE.

A composite video signal for a white picture, with sync. pulses positive, and with amplitudes as in Fig. 11a, is fed into the clamp circuit of Fig. 8a. The voltage waveform across the total resistance (Fig. 11b) adjusts so that the positive area is 0.02 times the negative area. This occurs when the sync. pulse extends an average of 2.45V positive, as can be verified by calculation of the waveform areas.

When the voltage lost across the source resistance is now taken into account, only one tenth of the positive amplitude appears at the output but almost all (1/1.018) of the negative amplitude is output.

The average amplitudes of the output waveform are as shown in Fig. 11c. Remember that the waveform shown indicates average values only and that the actual waveform has a tilt on the normally horizontal sections of the input waveform. The important point about the average output voltage is that the sync. pulse amplitude has been greatly reduced, making the blanking level much closer to zero than it should be. There is little reduction, however, in the amplitude of the picture information section of the waveform.

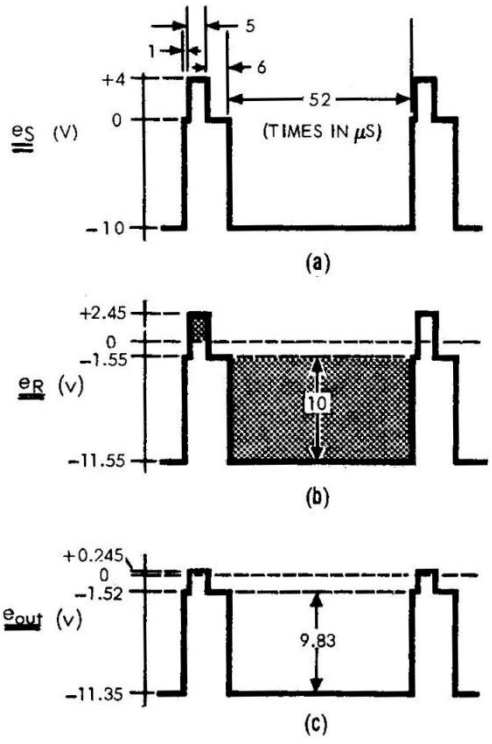


FIG. 11. AVERAGE VOLTAGE FOR COMPOSITE VIDEO SIGNAL.

2.8 The best way to avoid the large reduction in sync pulse amplitude by clipping of the peaks of the input signal, is to increase the ratio of the discharge to the charge time constant by increasing the value of the shunt resistance (R_1) in the clamp circuit. This reduces the amount of discharge of the capacitor when the diode is non-conducting, and also the tilt produced on the unclamped section of the waveform. Less current is required, therefore, to recharge the capacitor when the diode conducts, and the total resistor voltage does not extend as far into the positive region. The improvement produced by increasing R_1 is partly offset by an increase in the diode forward resistance (R_f) because of the reduction in diode forward current.

In Fig. 12a. The discharge time constant of the capacitor is increased ten times to 100mS by increasing the shunt resistance to 1MΩ. Ignoring any change in diode forward resistance, the ratio of the charge to discharge time constants, and therefore, the ratio of the positive area to the negative area of the waveform across the total circuit resistance for this clamp circuit, is 0.002. The average voltage across the total circuit resistance and the average output waveform for this condition are shown in Figs. 12c and d. Note that the reduction in the amplitude of the sync. pulse is not nearly as great as the reduction in Fig. 11.

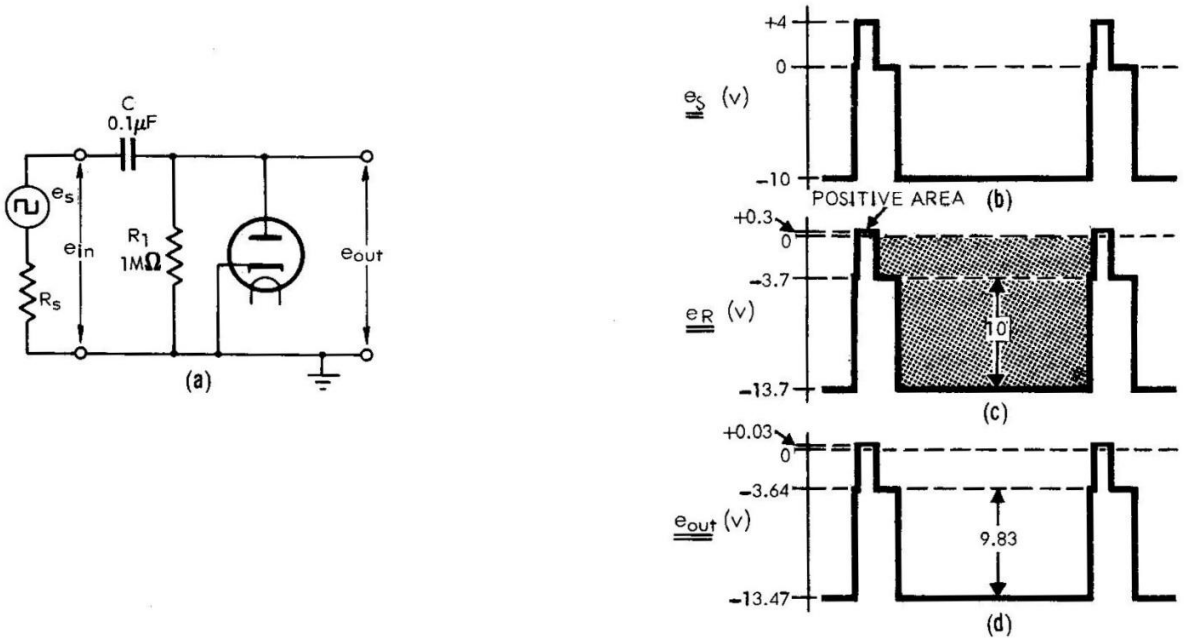


FIG. 12. AVERAGE VOLTAGES WITH INCREASE IN SHUNT RESISTANCE.

An important point related to pulse duration and clamping level is that, as the pulse duration changes, so also does the clamping level change. In particular, with a television composite video signal input the blanking level shifts with the change in the pulse duration that occurs during the vertical sync. pulse period. The broad pulses of the video signal are more accurately clamped than the horizontal sync., and equalizing pulses and blanking level during the vertical sync. period appears to be shifted towards white. The magnitude and duration of the shift of blanking level depends on the charge and discharge time constants of the clamp circuit.

2.9 Effect of Pulse Amplitude. When the output waveform from a peak rectifier clamp is not established finally at the reference voltage, the deviation of the output from the clamp voltage depends on the amplitude of the input signal. An important practical example of the variation of the amplitude of the input signal occurs in television applications where the picture signal amplitude of the composite video signal depends on the picture being scanned. The dependence on signal amplitude is indicated by examining the operation of the positive peak rectifier clamp in Fig. 8a, where the shunt resistor is 0.1MΩ when the composite video signal input corresponds to a black picture, (Fig. 13a), instead of a white picture as in Fig. 13.

When the positive area is 0.02 times the negative area of the output waveform, the average amplitude of the voltage across the total resistance (Fig. 13b) extends to +0.9V and the sync. pulse tips of the output waveform extend to +0.09V. The output waveform in Fig. 13c shows that the blanking level is at -3.05V when the video signal contains black picture information, but with white picture information the blanking level was at -1.52V (Fig. 11c).

If this change in the blanking level with picture signal is communicated to the picture tube, the picture displayed will not reproduce the original shades correctly (but will be much better than if the signal was A.C. coupled without and D.C. restoration). The clamping provided by this circuit is not adequate for television transmission equipment.

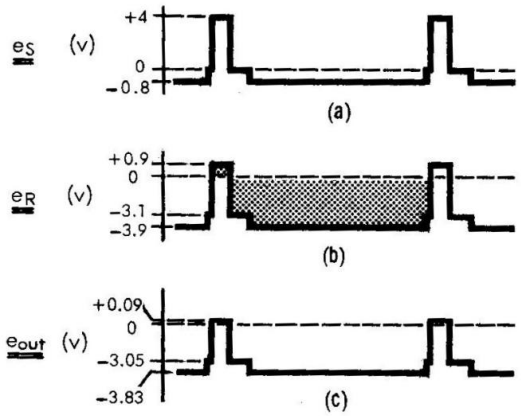


FIG. 13. AVERAGE VOLTAGES FOR COMPOSITE VIDEO SIGNAL.

When the discharge time constant is increased by a factor of ten as in Fig. 12, the variation of the blanking level is less dependent of the signal voltage. The blanking level changes from -3.64V (Fig. 12) to -3.82V with the change from a white to a black picture signal.

The dependence of the clamping level on the amplitude of the input signal can be reduced by returning the shunt resistor to a stabilising bias voltage as in Fig. 14. This does not change the clamping reference level as did the bias considered in para. 2.4. During the time when the diode is conducting, the stabilising bias voltage does not affect the charge on the capacitor, but during the non-conducting time, the capacitor discharges towards the stabilising bias potential. With a stabilising bias much greater than the signal level, change of signal level has negligible effect on the discharge current, and therefore the charge current with the diode conducting is not changed, and clamping level and loss of amplitude in the source resistance are independent of signal amplitude.

Though the clamping error does not vary, it is larger than it would be without the bias, being a proportion of the bias potential instead of a proportion of the signal level. To reduce this larger error and to retina a tilt on the unclamped section of the output waveform having the same order as is obtained with the unbiassed circuits, the value of shunt resistance must be increased.

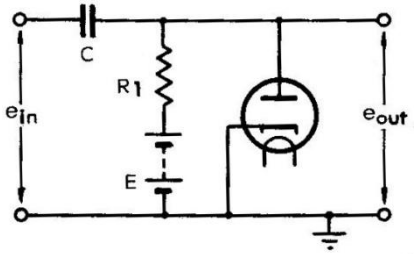


FIG. 14. CLAMP CIRCUIT WITH STABILISING VOLTAGE.

2.10 Recovery Time of Clamp Circuit. To examine the recovery time, consider a 100V p-p 500c/s square wave generator voltage in the peak rectifier clamp of Fig. 8a. The repetitive output waveform is as shown before time t_x in Fig. 15b. A D.C. shift of 25V in the negative direction is introduced on to the source square wave at time t_x in Fig. 15a, the commencement of a positive half cycle, and the voltage across the total resistance steps by 75V to -15.48V. The diode, therefore, does not conduct and the majority of this voltage (-15.21V) appears at the output. The resistor voltage decreases exponentially towards zero and reaches 14.01V during the positive half cycle. The total resistor voltage then steps negatively by 100V to -114.01V and again decays exponentially towards zero. During this cycle of the input, no clamping occurs as the complete waveform is negative with respect to the clamp potential. The average axis of the resistor voltage drifts exponentially in a positive direction until the positive extreme of the resistor voltage exceeds the clamp reference voltage, and then clamping recommences. The time constant of the vertical shift of the waveform is long because the diode is non-conducting, and the clamp action is lost for a time related to this time constant. During this time the capacitor charge gradually changes between values dependent on the D.C. components of the two sections of the input signal. A change in the clamped level at the input by a change in signal amplitude produces a similar effect.

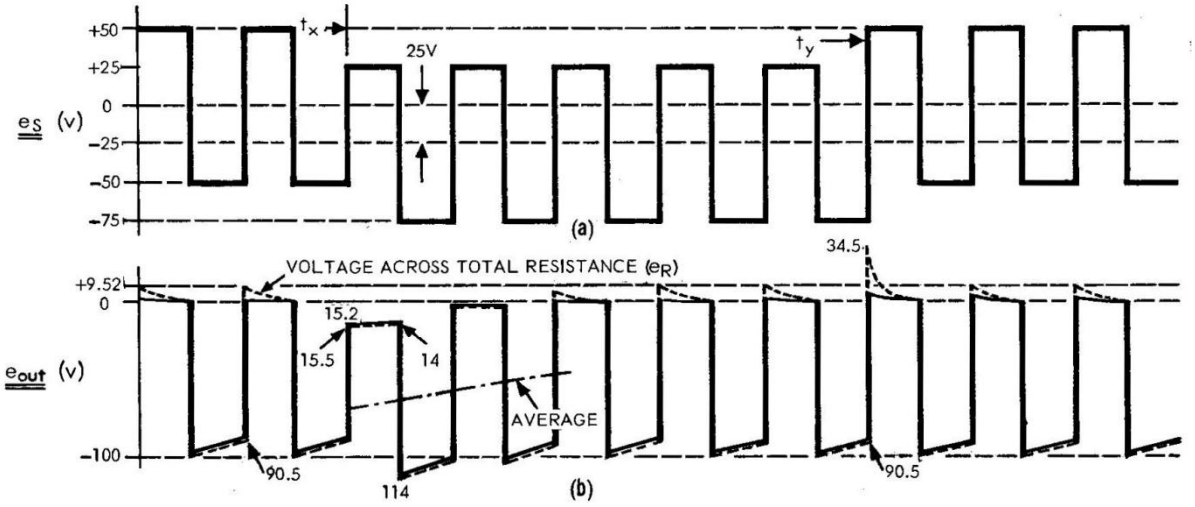


FIG. 15. SHIFT OF LEVEL TO BE CLAMPED.

When the positive extreme of the input signal is shifted in a positive direction by an increase in amplitude, or a positive change in the D.C. component as at t_y in Fig. 15a, the clamping action is not lost. With the shift of the extreme of the signal, the diode is driven heavily into conduction and the capacitor charges quickly to the new voltage required for correct D.C. restoration.

Fig. 15 shows that, for changes in voltage of the level to be clamped, the peak rectifier clamp corrects more quickly in one direction than in the opposite direction. It can only clamp when the signal level errors cause diode conduction. This circuit is therefore described as being a one-way clamp. Negative peak rectifier clamps have opposite characteristics.

2.11 Input Signal Tilt. Preceding paragraphs considered rectangular wave input signals. However, the main reason for requiring a clamp circuit is that the D.C. component has been lost, for example, by passing through an A.C. coupling circuit. This circuit will introduce onto the input signal a tilt dependent on the time constant of the components. Consider a section of a composite video signal for a black and white picture containing tilt (Fig. 16a) as is produced by attenuation and leading phase shift at low frequencies. This signal is the input to a peak rectifier clamp, and at the output the sync. pulse peaks are established at the reference potential during the sync. pulse time, as at time t_1 in Fig. 16b. With a discharge time constant for the circuit much longer than the line time, the clamp circuit introduces only a small additional tilt on the white signal during the line following t_1.

Because of the original and the added tilt, the next sync. pulse again causes the diode to conduct, so returning the sync. tip to the clamp reference potentials. This process continues until time t2. Now the tilt on the input signal is negative. The clamp circuit causes a slight reduction of this tilt, but with a long time constant, only a small change occurs and the next sync. pulse is not capable of causing diode conduction to produce clamping. This situation persists for the complete white section of the signal and for some of the following black section and is another illustration of the one-way clamp action of the circuit.

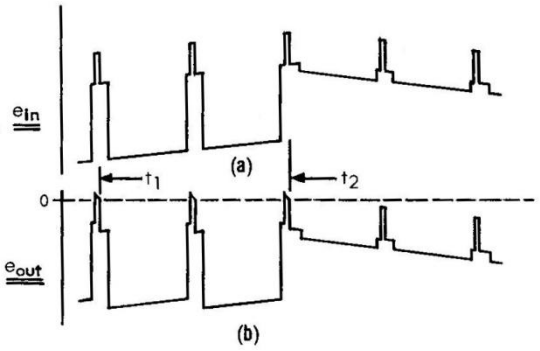


FIG. 16. INPUT SIGNAL TILT.

For clamping to be maintained in the presence of input signal tilt, the time constant of the circuit between clamping times must be reduced so that sufficient tilt is introduced to "cancel" the negative tilt of the input signal. Then the diode can conduct on each sync. pulse. Stated another way, the time constant must be shortened so that the capacitor voltage can follow input variations of the level to be clamped. The same applies for input level variations caused by interference instead of by the low frequency characteristic of preceding equipment. The discharge time constant required to maintain clamping is dependent on the tilt and the signal level, but for a particular case of 20% tilt on a 50c/s square wave composite video signal varying between black and white, the time constant must be less than 20mS. The peak rectifier clamp is slightly less conscious of the opposite tilt as is produced by increased amplitude and lagging phase shift at low frequencies. Since the peak rectifier clamp requires a long discharge time constant to give accurate clamping with minimum tilt between clamping times, it is not suitable for clamping signals with large degradations.

2.12 Effect of noise. One major disadvantage of peak rectifier clamps is that they are not immune to noise. When a noise pulse occurs during the clamping time or if a noise pulse occurring at any other time is of sufficient amplitude to exceed the clamping level, the capacitor of the clamp circuit attempts to charge to the amplitude of the noise pulse. This shifts the signal from its correct clamping level and the recovery time depends on the long time constant of the circuit with the diode non-conducting. The effect is indicated by the waveform in Fig. 17.

Reducing the discharge time constant of the circuit reduces the recovery time following clamping to a noise pulse, but tilt and clamping are increased.

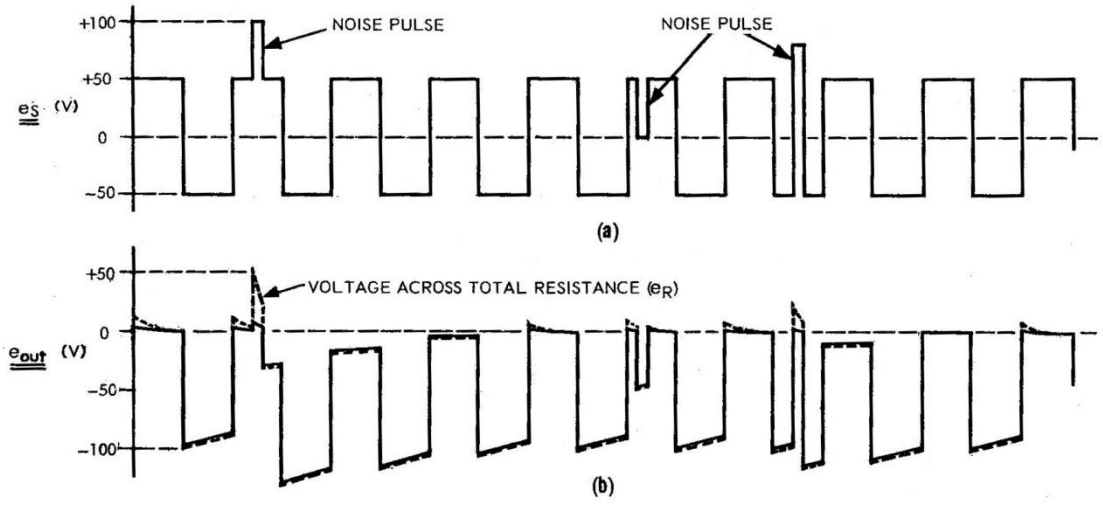


FIG. 17. EFFECT OF NOISE.

Noise immunity can be improved by increasing the charge time constant of the capacitor. This makes the circuit slower acting to changes in level in the direction which otherwise has a fast recovery time. A resistor in series with the diode across the output is usually preferred, as this increases the charge time constant without increasing the clipping in the source resistance. Improved noise immunity is achieved by using the circuit in Fig. 18. Here the A.C. component of the signal is coupled via C_1 to the output. From the same input a D.C. component is derived in a peak rectifier clamp comprising C_2, R_1 and V_1. This D.C. component is filtered in a long time constant circuit (R_2, C_3) to remove the original signal, and in addition any fast change of D.C. component as would be produced by input noise. The D.C. component is then fed to the output via R3. The filter circuit gives the circuit a slow acting characteristic for both directions of shift of the level of the input signal to be clamped.

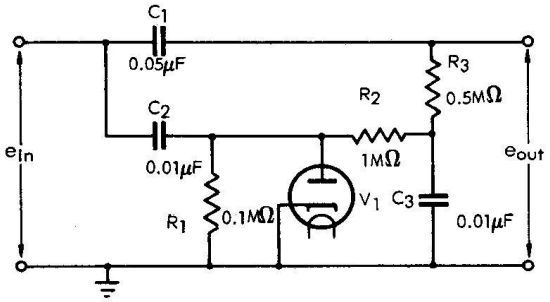


FIG. 18. FILTERED D.C. RESTORER CIRCUIT.

2.13 Grid-Cathode Circuit Clamping. The grid-cathode circuit of multi-element tubes such as triodes and pentodes is often used in place of the diode in the preceding peak rectifier clamp circuits. A circuit is shown in Fig. 19a. The positive extreme of the grid signal is clamped to the cathode potential, and the circuit introduces a negative D.C. component on to the grid signal, thus providing bias for the tube. The circuit is identical with one usually called a grid leak bias circuit. In oscillator circuits and transformer coupled amplifier circuits, the resistor is often directly across the capacitor, but this gives the same clamping action. In pulse circuits the grid resistor is commonly connected to H.T. as in Fig. 19b. This is equivalent to the clamp circuit with stabilising bias in Fig. 14. Because of the high value of resistance (R1) used, little grid current flows and the tube is not damaged.

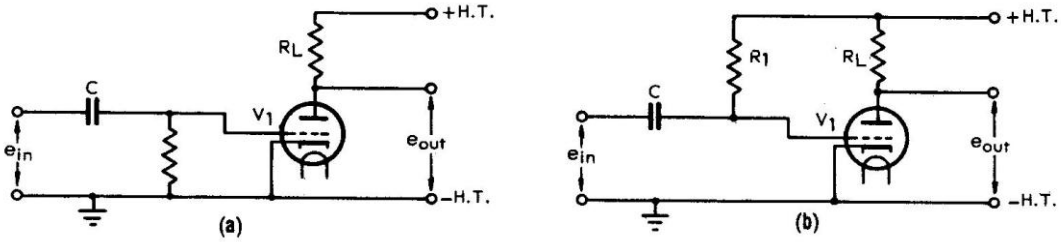


FIG. 19. GRID-CATHODE PEAK RECTIFIER CLAMPS.

Usually the grid-cathode circuit of multi-element valves represents a higher resistance than the anode-cathode resistance of diodes, and it does not provide accurate clamping. When clamping is achieved with a triode or pentode, the valve acts as a D.C. amplifier, the output voltage at the anode is inverted, and the negative extreme of the signal is clamped to a low anode voltage. This voltage is dependent on the value of anode current with zero bias voltage, and on the anode load resistance.

The most common use for clamping in multi-element tubes is in television waveform sync. separation. The sync. tips of the composite video signal are clamped to the cathode potential and the signal is of sufficient amplitude to cause the negative going picture information to drive the grid beyond cut-off. Therefore, the output waveform contains only the synchronising information.

2.14 Conclusions. In paras 2.5 to 2.12 the circuits were "poorly designed" to exaggerate the defects of peak rectifier clamps. A number of interacting requirements for the values of the components of clamp circuits are illustrated. These are summarized as follows:-

- The resistance of the conducting diode (R_f) must be low compared with the source resistance, to prevent the clamped level from deviating far from the clamp reference potential.

- As the diode resistance decreases with the increase in diode current, the signal input voltage should be high.

- The source resistance should be low to prevent loss in this resistance when the diode conducts, thereby changing the relative levels of the signal. Also, a low source resistance decreases the charge time of the capacitor with the diode conducting. When the charge time constant of the capacitor is not less than 0.2 of the clamping time, the output is not clamped finally to the reference potential, and the actual clamping potential varies with change of clamping time and with change of amplitude of the input signal, particularly when the discharge time constant (CR_1) is not long.

- The time constant of the circuit capacitance and the shunt resistance (CR_1) should be long, to give negligible tilt, accurate clamping, and negligible loss in the source resistance. This, however, makes the circuit slow to recover in one direction when the input signal has a changing D.C. component, a changing amplitude or noise. A relatively short time constant (CR_1) improves the recovery time, but introduces changes in the relative signal levels, tilt, and inaccurate clamping.

In practice a compromise must be decided on depending on the characteristics required. Typical values of time constant for television applications, where the clamping time at the sync. tips is approximately 5µS every 64µS, are:-

(i) For circuits designed to be slow acting, for use where the signal is to be established at a reference level but large signal degradations are not present. — 0.02-0.1 sec.

(ii) For circuits designed to be fast acting, for use where rapid variations of the signal level to be clamped occur at the input. — 0.002-0.01 sec.

The main advantages of peak rectifier clamps are that they are simple and cheap. They are not suitable, however, where accurate or fast acting clamping is required.

The disadvantages of the circuits are:-

(i) Clamping can only be achieved on peaks of the signal.

(ii) For television the amplitude of the sync. pulses and set-up must be accurately maintained for black level to be established at a fixed level.

(iii) The circuits are one-way clamps and correct for changes in one direction much faster for changes than in the other.

(iv) They are susceptible to "noise" pulses even those of short duration.

(v) Accurate clamping is not possible in fast acting circuits.

The peak rectifier clamp, as discussed in this Section, gives some measure of suppression of low frequency interference, and compensation for errors in low frequency characteristics. However, because of its disadvantages, only small errors can be corrected, and it is rarely used for this purpose in video transmission equipment. Its application is limited mainly to the clamping of pulse waveforms, and to the restoration of the D.C. component to video signals, when low frequency response is adequate and when the amplitude of any interference is small.

3. KEYED CLAMP CIRCUIT PRINCIPLES.

3.1 Advantages. Most of the disadvantages of simple peak rectifier clamps can be overcome by using "keyed", "gated" or "driven" clamp circuits in which the clamping action takes place only at a time when "keying" or "gating" clamp pulses are present. Keyed clamp circuits are of major importance in television transmission equipment as they have the advantage of being:-

(i) Fast acting for input signal changes in both directions - they are two-way clamps.

(ii) Able to clamp accurately to a specific level.

(iii) Satisfactory for clamping signals of relatively small amplitudes.

(iv) Capable of achieving clamping on any section of the wave that is repetitive. For television this means that clamping can be achieved to blanking level in the "back porch" period. Black level is then only dependent on the adjustment of the set-up and not on the sync. Pulse amplitude.

(v) Able to be used for clamping video signals of both polarities (that is, signal with either positive or negative picture signals) without alteration of the circuit.

(vi) More immune to noise than the peak rectifier clamp because clamping can occur only during the short time of the clamp pulse.

3.2 Clamping of Video Signals. As keyed clamp circuits are used mainly in television equipment, descriptions of circuits are related to television video signals. In the majority of television applications, clamping occurs during the back porch period, when blanking level is clamped to a reference level. The duration of the back porch of a composite video signal conforming to the Australian standards is approximately 5.5µS (4.8 to 6.2µS but not directly specified). Clamp pulses are produced with durations so that they occur only during this time. Typical clamp pulses are developed by triggering circuits from the trailing edge of the sync. pulses. They are normally delayed by 0.5 to 1µS from the conclusion of the sync. pulses, and have durations of 1 to 3µS. In some cases, composite video signals are clamped at the top of the sync. pulses, and in these cases amplified sync. pulses may be used as clamp pulses. Clamping to sync, tips for D.C. restoration is only satisfactory when the sync. pulse amplitude does not vary. Non-composite video signals can be clamped at any time during blanking intervals. The following discussion centres on clamping composite video signals, during the back porch period.

3.3 Principle of Keyed Clamp Circuits. Fig. 20 shows a basic keyed clamp circuit. The clamp switch is arranged to be closed during the clamping period, and this connects the output terminal directly to the clamp reference potential. In practical circuits an electronic switch is used instead of the contact shown. The output is connected to a very high impedance circuit, usually directly to the grid of a valve. The circuit operates ideally when no shunt resistance exists across the output. This is in contrast to the peak rectifier clamp in which resistance is necessary if the circuit Is to be capable of correcting for both directions of change of the input level to be clamped. In practical keyed clamp circuits a high value of resistance of the order of 10MΩ is sometimes included across the output to prevent problems associated with grid current in the valve. This is rarely necessary in low power television circuits when clamping occurs at the line frequency.

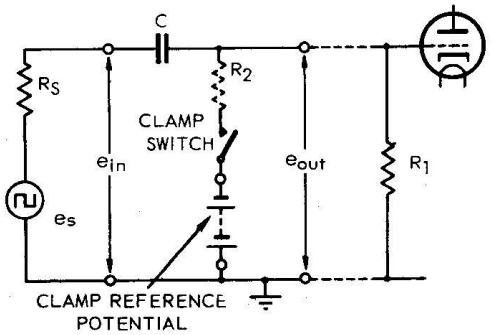


FIG. 20. BASIC KEYED CLAMP CIRCUIT.

With an input signal to the basic keyed clamp circuit, such that the signal blanking level during the clamping time is at the clamp reference potential, no error exists and no current passes through the clamp switch.

When the input signal during the clamping time is not at the correct level, the closing of the switch allows a current to charge the capacitor towards the error voltage. The charged capacitor voltage provides a correcting voltage to compensate for the error in the voltage of the clamped section of the waveform. It does not matter whether the error is positive or negative, that is, whether the level to be clamped is positive or negative with respect to the clamp reference potential, the charge on the capacitor adjusts itself suitably.

The time constant of the charge circuit of the capacitor in Fig. 20 is the product of the capacitance (C) and the source resistance (R_S), but it a practical circuit some resistance exists in the switch. Ideally the circuit resistance and capacitance should be selected so that the capacitor is completely charged to the error voltage in the time for a clamp pulse, but because of the short duration of the pulse, a sufficiently short time constant is hard to achieve. Satisfactory clamping is achieved if the capacitor is able to charge to 90% to 95% of the error voltage during one clamping time and often less error correcting than this is acceptable.

The value of the capacitor (C) is normally much smaller than that used in coupling circuits for video signals. A typical value is 1000pF. This is possible because, when the clamp switch is opened, a very high or even infinite resistance appears across the output, and also because it is only necessary to design the time constant of the capacitor discharge circuit so that negligible tilt is produced between clamp pulses which have a frequency of 15,625c/s for television signals.

3.4 Details of Clamping Action. Consider a composite video signal fed into a keyed clamp with no initial capacitor charge and with zero clamp reference voltage. The amplitude of the blanking level during the back porch interval is +0.1V. Details of the circuit waveforms during the back porch time are shown in Fig. 21.

Prior to clamping the output voltage (e_{out}) is +0.1V since no voltage exists across the uncharged capacitor. When the switch closes the output voltage falls immediately to zero (if the switch is considered as having zero resistance) and remains at zero for the duration of the close period.

Since there is no charge on the capacitor, at the instant the switch closes the input voltage (e_{in}) must also fall to zero. This means that the total source voltage (e_S) is dropped across the source resistance (R_S). During the clamping time a current flows to charge the capacitor (C) and the input voltage (which equals the voltage across the capacitor when the switch is closed) rises towards the 0.1V error voltage. Consider that in the clamping time the voltage rises to 90% of the final voltage and at the end of the clamping time the input voltage and capacitor voltage is 0.09V. When the switch opens, the source voltage blanking level error of 0.1V still exists. With no current through the source resistance this error appears at the input, but because of the charge on the capacitor the output voltage is 0.1-0.09V = 0.01V. The error in blanking level has been reduced to 10% of its original value.

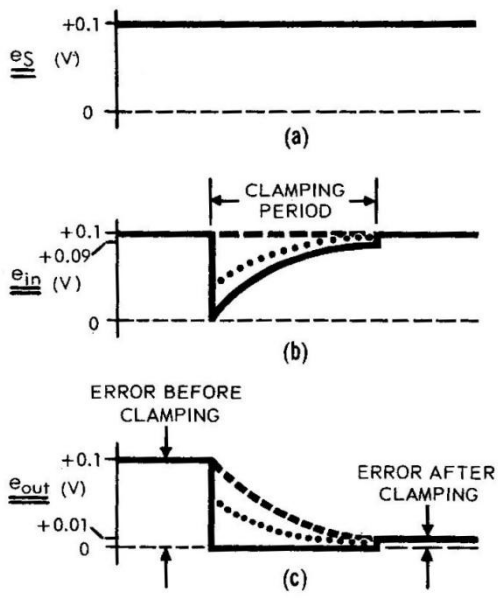


FIG. 21. CLAMP CIRCUIT WAVEFORMS.

During the next clamping period, if the source voltage error has not changed, the remaining error of 0.01V is reduced again to 10% of this value. Therefore, even when the capacitor is not completely charged in the clamping time, very accurate clamping is possible after several closures of the clamp switch. When the time constant of the capacitor charge circuit is such that the capacitor can be completely charged in one clamping period, no error exists after this time. Notice in the output waveform shown in Fig. 21 that a "notch", with a magnitude dependent on the error to be corrected, can be produced in the back porch during the clamping time even with a perfect switch.

When the switch circuit contains some resistance, the output does not fall immediately to zero. During clamping a proportion of the total resistor voltage is present across the clamp switch circuit and the circuit waveforms are as shown dotted in Fig. 21. The size of the notch depends on the relative values of the switch resistance and the source resistance.

When the source resistance is zero the notch disappears, and the output waveform changes exponentially from one value to another during the clamping time, as shown with the dashed line in Fig. 21.

In practical circuits resistance is sometimes added in series with the clamp switch to "soften" the action of the clamp so that a minimum amount of waveform degradation is introduced. Remember, however, that adding resistance in the capacitor charge circuit increases the charge time constant of the capacitor, and reduces the percentage that the error in the signal level is corrected in one clamping period.

To some extent, the resistance in series with the clamp switch isolates any switch capacitance present during the unclamped time from the video circuit, and therefore reduces the effect on this capacitance on the high frequency components of the input signal.

"Softening" of the clamping action is often used when clamping colour television composite video signals with the reference colour sub-carrier (colour burst) in the back porch. This is to prevent this colour burst from being affected by the clamping action, and to prevent the circuit from attempting to clamp to the varying potential of the colour burst. An improved method of preventing the colour burst being affected is to add a damped parallel resonant circuit tuned to the colour sub-carrier frequency in series with the clamp switch. Thus a high impedance is present in the switch circuit only at the colour burst frequency, and normal clamping to the average amplitude is achieved without distortion of the colour burst. The resonant circuit is usually shunted by a resistance to reduce its Q so as to prevent ringing at the colour burst frequency.

It is extremely important that the clamp switch be opened before the end of the back porch period, or the circuit will attempt to clamp to the incorrect level. Also, if the clamp switch closes before the commencement of the back porch time in the sync. pulse time, the circuit will attempt to clamp to the incorrect level, but this effect will be cancelled as long as the switch is still closed for a considerable portion of the back porch time. However, unnecessary degradation of the sync. pulse and back porch will occur.

3.5 Clamping of Signal Containing Interference. Once the charge has been established on the capacitor, and since no discharge path exists, this fixed amount of level correction must persist until the next clamping time. Therefore clamping cannot correct for errors that exist during the line period. This is illustrated by examination of the clamp circuit when the input signal is a composite video signal combined with a sine wave interfering signal as in Fig. 22a.

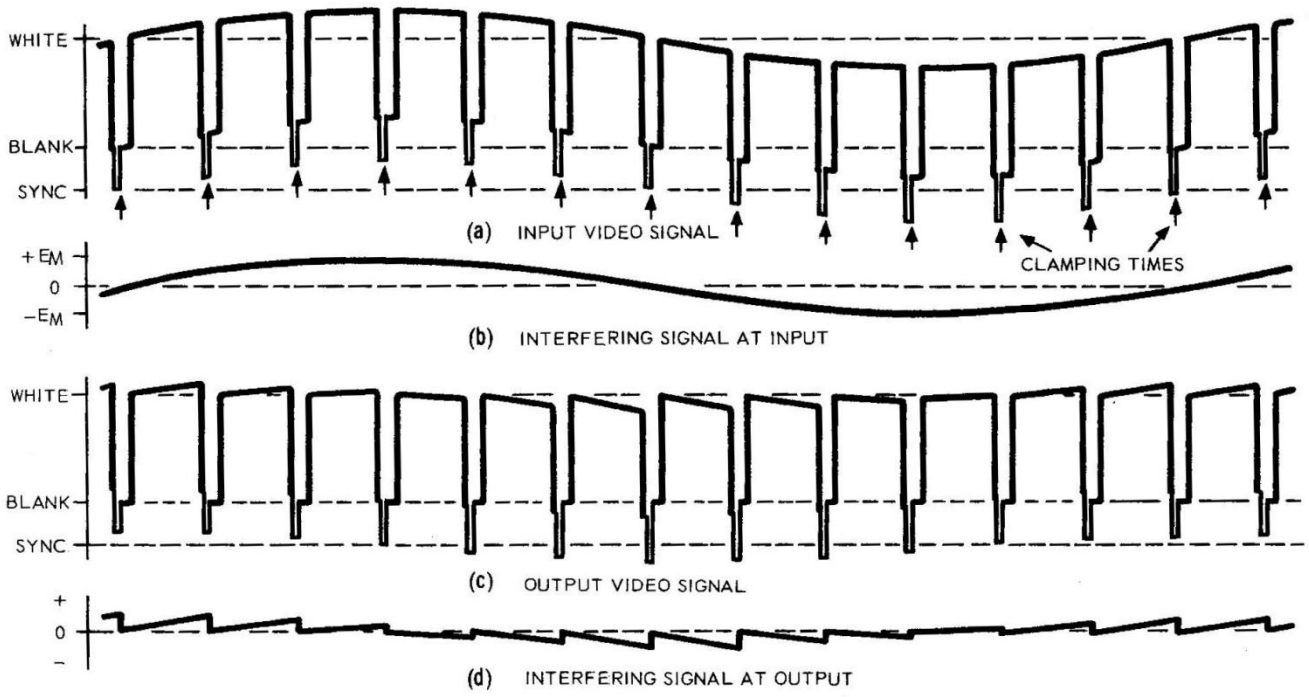


FIG. 22. CLAMPING VIDEO SIGNAL CONTAINING INTERFERENCE.

Details of the waveform during the back porch have been simplified by considering that error correcting occurs instantly, coincident with the trailing edge of the sync. pulse. Fig. 22c shows that the clamped vision waveform between clamp pulses is unchanged, and that significant tilt is present in this example where the clamping rate is only 12 times the interfering signal frequency. For lower frequency interfering signals, level change during the line time is correspondingly smaller. In television practice most of the large amplitude interfering signals are either 50c/s or the ripple frequency of the equipment power supplies. For an interfering signal with a magnitude as in Fig. 22b, but with a frequency of 50c/s, the maximum line tilt is approximately 1/26 of the maximum of Fig. 22c. A peak-to-peak 50c/s interfering signal amplitude equal to the peak-to-peak video signal amplitude can be satisfactorily eliminated by clamping.

The interfering signal component of the resultant video signal in Fig. 22c is illustrated in Fig. 22d. This component is a maximum when the rate of charge of the original interfering signal is a maximum; that is, as the original sine wave passes through the zero axis.

Consider a 50c/s interfering signal with a peak-to-peak amplitude of 1V superimposed on a composite video signal. The maximum rate of change of the interfering signal is:-

$$E_M \times 2\pi f$$

$$= 0.5 \times 2 \times 3.14 \times 50$$

$$= 157 \text{ V/Sec.}$$

Clamp pulses occur every 64µS, and during this time the interfering signal varies a maximum of:-

$$\frac{157 \times 64 \times 10^3}{10^6}$$

$$= 10\text{mV}$$

This 10mV is the peak amplitude of the resultant interfering signal, if the capacitor charge times and the clamping times are negligible. Since the line tilt is in opposite directions for positive and negative going sections of the original interfering signal. The resultant signal contains an interfering signal of 20mV peak-to-peak. This is 1/50 of its original value, and a reduction in peak-to-peak amplitude of approximately 34db.

The maximum rate of change of a sine wave is proportional to frequency. Therefore, for a given amplitude, as the interfering signal frequency is increased, the maximum tilt during any line increases, and the amount of interference suppression decreases. The amount of suppression is approximately inversely proportional to the interfering signal frequency, when this frequency is much less than the clamping frequency.

3.6 The peak-to-peak amplitude of interfering signals, with frequencies approaching and above half the clamping frequency, can be increased by up to 6dB by the action of a clamp. An interfering signal with a frequency equal to half the clamping frequency is illustrated in Fig. 23a, with the clamping times indicated by arrows. The resultant interfering signal after clamping (Fig. 23b) shows that the voltages at both positive and negative peaks are established at the clamp reference potential by clamping action. This waveform has a peak-to-peak amplitude twice that of the original interfering signal, representing a peak-to-peak increase of 6db. However, no change in the interfering signal level occurs when a change in relative phase causes the clamping times to be as indicated by the circles in Fig. 23a. For other high frequency interfering signals at the input, the output contains a beat with a frequency equal to the difference between the input interfering signal frequency, and the clamping frequency.

Less increase in the amplitude of high frequency interfering signals is produced by keyed clamping when the charge time constant for the clamp capacitor is increased. An increase in this time constant, however, reduces slightly the effectiveness of clamping when the input signal includes low frequency blanking level variations.

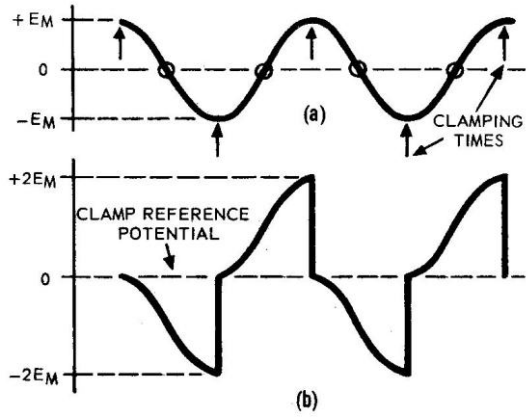


FIG. 23. CLAMPING OF HIGH FREQUENCY INTERFERENCE.

3.7 Effect of Noise. The effect of random noise on keyed clamp circuits is smaller than its effect on peak rectifier clamps, because only noise occurring during the clamping time, can alter the clamping level. When noise occurs during the clamping time, the blanking level is incorrectly established and this incorrect level will persist for the following line period. Therefore streaking, produced by clamping to the noise, can result in a worse picture than that produced by the noise signal alone, before clamping. To reduce the effect of noise, the clamping time is made as short as practicable. Also the charge time constant of the clamp circuit is sometimes deliberately lengthened to soften the clamping action so that it takes many clamping times to correct for a blanking error. The circuit clamps to the average blanking level of several consecutive blanking periods.

A more disturbing effect than clamping to the noise in the back porch period is produced when the noise causes false triggering of the clamp pulse generator. This malfunction can produce clamp pulses during the active line time, and so cause the picture signal at this time to be clamped to the reference potential. False generation of clamp pulses by noise can be eliminated by including a "flywheel" type of sync. separator before the clamp pulse generator. In this type of circuit, gating signals are generated to control the sync. separator, so that an output can occur only during sync. pulse times.

3.8 Practical Waveforms. Fig. 24 shows waveforms photographed from a C.R.O used to monitor the input and the output of a keyed clamp circuit. The composite video signal is for a black picture, and the interfering signal is a 100/c/s sine wave.

With the C.R.O. time base set to display approximately one filed, the large amplitude interference at the input is shown to be reduced at the output. Notice that the maximum amplitude of the output interfering signal coincides approximately with the maximum rate of change of the input interference signal, as discussed in para. 3.5. When the C.R.O. time base is set to display approximately one line, many lines of the complete picture are superimposed. The input signal waveform (Fig. 24) includes a large amount of "broadening" of the horizontal sections. The "broadening", which is caused by the interfering signal, is considerably reduced at the output. The tilt introduced by the interfering signal during the line time, is indicated by the slight increase in the "broadening" of the trace towards the end of the line.

In this example clamping is carried out for the complete back porch period, but because of the clamp switch resistance and the value of the series clamp capacitor, the decrease in the blanking level error in one back porch period is only 25% approximately. This is indicated by the slight reduction in the trace "broadening" towards the end of the back porch period. With this order of error reduction per clamping time it would take approximately 17 lines for an error to be reduced to 1% of its initial value. The slow rate of error reduction is responsible for the rather small reduction in the interfering signal amplitude of approximately 6:1 (≈ 16db) achieved in this circuit compared with the theoretical maximum reduction of approximately 28db with a 100c/s interfering signal. The "soft" clamping action, however, does not cause much degradation of the waveform during the back porch time. When the complete blanking level error is removed during the clamping time, the "broadening" of the trace is reduced to zero in this time.

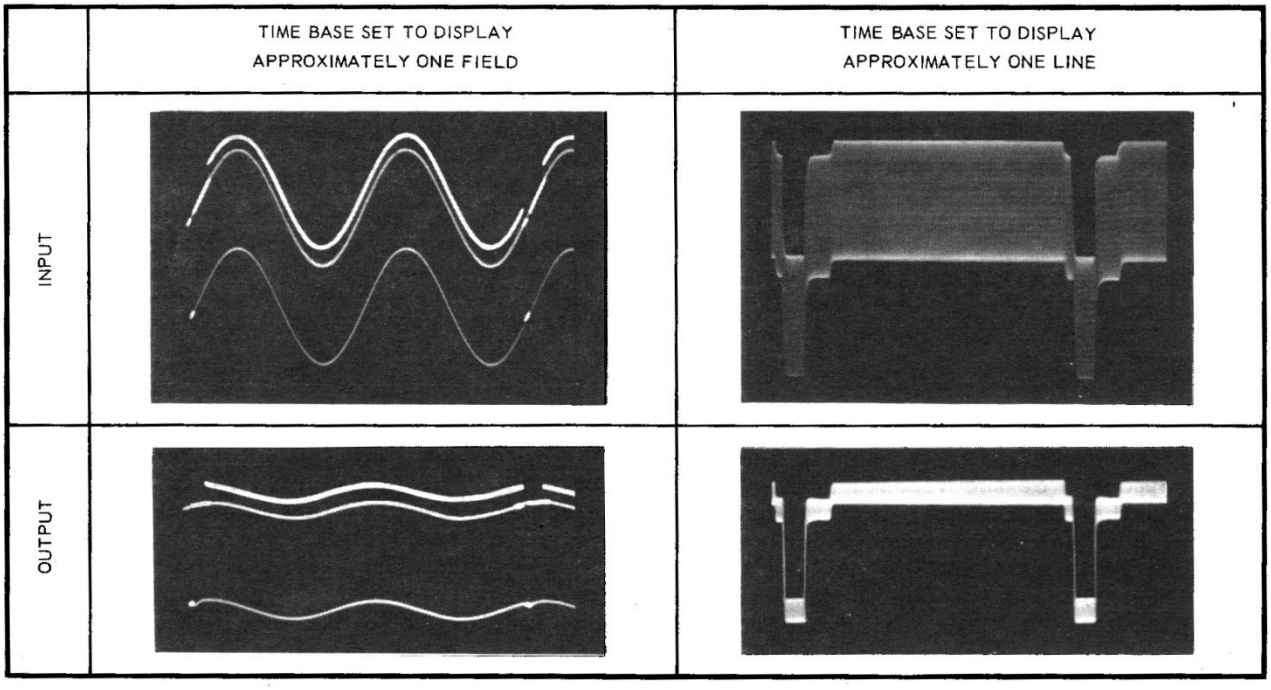


FIG. 24. REDUCTION OF INTERFERENCE BY CLAMPING.

The clamp circuit is equally effective for removing tilt due to amplitude and phase errors at low frequencies, for removing transient interference caused by switching producing a temporary shift of the D.C. level of the signal, and for inserting a D.C. component. Since the back porch can be fixed at any level, the clamp reference potential can be used to provide the correct bias for the amplifier stage following the clamp circuit.

3.9 Feedback Clamp Circuit. The keyed clamp circuit of the series capacitor type as considered in paras. 3.3 to 3.8 has a disadvantage. Because the series capacitor keyed clamp must be followed by a circuit with a high D.C. resistance, and video amplifiers are required with low impedance outputs, at least one amplifier stage is required between teh clamp circuit and the output. To maintain the restored D.C. component between the clamp and the output a D.C. amplifier is used. The output is then not accurately fixed at the reference potential, as the amplifier stage can produce long term drift of the clamped level at the output. The necessary high resistance input is difficult to achieve in transistor circuits, and is made more so, since a D.C. amplifier with a small amount of drift of output level is required. An increase in the signal level reduces the percentage variation of the clamped level, but makes it harder to achieve adequate linearity in the amplifier stage.

This disadvantage can be eliminated by using feedback techniques. Fig. 25 shows a block schematic of a typical arrangement. The output signal is sampled during the back porch period by switch S_1 and pulses are derived that are dependent on the difference between the blanking level and the clamp reference level. These pulses are amplified in an A.C. coupled amplifier, detected by the synchronous switch S_2, and integrated so that a D.C. output is obtained with an amplitude proportional to the blanking level error at the output.

This error signal is introduced back into the video signal circuit in the correct phase to cancel the original error. Introducing the error via a cathode follower allows the correction to be made in a relatively low impedance circuit. The feedback can be connected to the output sampling point, or to an early stage of a D.C. video amplifier. Because of the gain in the feedback loop, very accurate clamping can be achieved right at the output terminals.

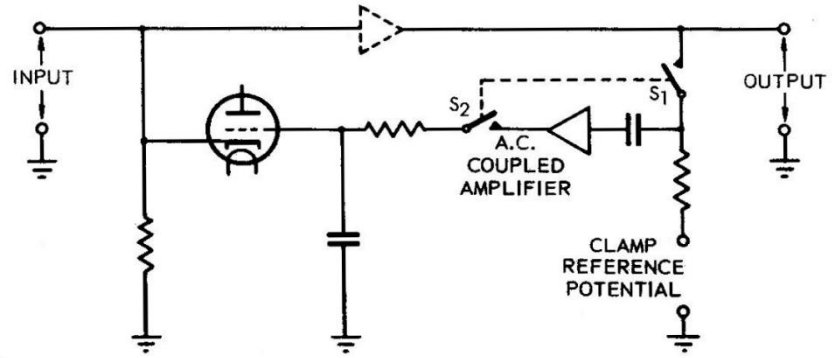


FIG. 25. PRINCIPLE OF FEEDBACK CLAMP CIRCUIT.

Picture monitors can use the feedback technique to advantage, to establish the D.C. component of the video signal at the picture tube. The blanking level is sampled, and the error signal is introduced into the control circuit via a feedback circuit with a time constant that is long compared with the filed time. The black level is correctly maintained on a long term basis, but degradations caused by low frequency interferences, or amplitude and phase errors at low frequencies are displayed in the picture. This feature is useful at programme monitoring points in a television transmission system, since it allows low frequency picture degradation to be displayed instead of being eliminated by the D.C. restoration circuits of the monitor.

3.10 The feedback principle is also used to stabilize the blanking level power output of vision transmitters. However, methods of deriving and inserting the error signals differ. A simplified block schematic of a blanking level feedback system for blanking level stabilization is shown in Fig. 26. Waveforms associated with the circuit are illustrated in Fig. 27.

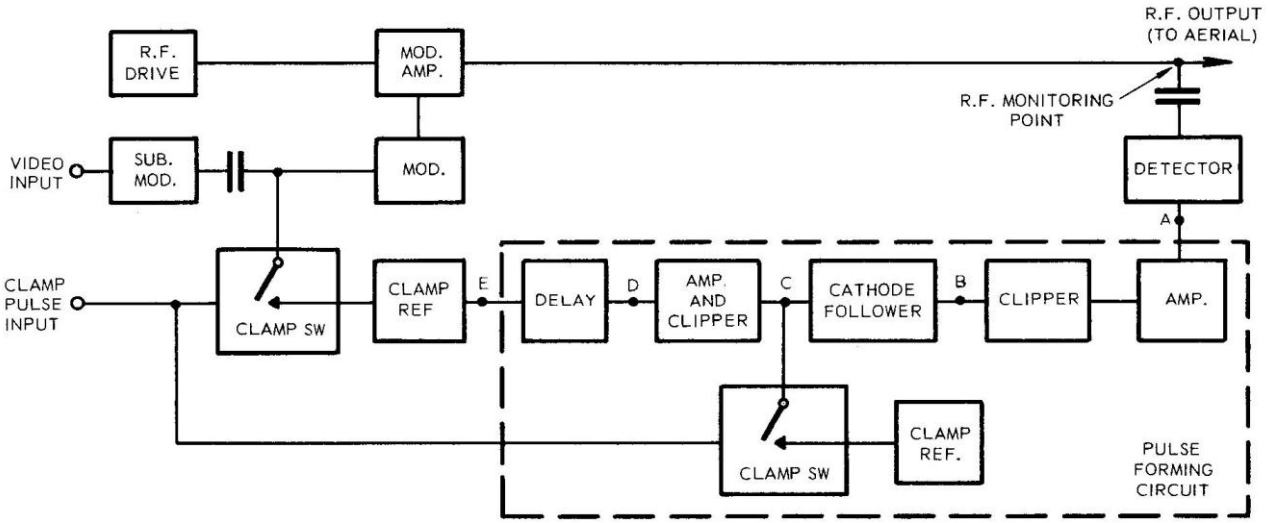


FIG. 26. BLANKING LEVEL STABILIZATION.

A signal from an R.F. monitoring point at the transmitter output is detected and the video signal, including the transmitted D.C. component, (waveform A), is recovered. The signal is inverted in the amplifier and the peaks of the sync. pulses are clipped at a fixed D.C. level to remove any sync. level variations. Blanking level variations then cause variations of the amplitudes of the resultant sync. pulses in waveform B. At C, following a cathode follower, blanking level is clamped to a reference potential using a keyed clamp circuit. Blanking level variations are thus transferred to become variations of level of the peaks of the sync. pulses. The clamp circuit provides bias so that the following amplifier conducts only during sync. pulses and removes the blanking and picture information to leave negative pulses (waveform D) coincident with the sync. pulses, but with amplitudes dependent on the transmitted blanking level. These pulses are delayed so that they occur during the back porch period (waveform E). They are then added to the clamp reference potential of a normal series capacitor keyed clamp at the input to the modulator. Blanking level at this point is therefore controlled by the transmitted blanking level. The modulator is direct coupled from its input to the gird modulated R.F. amplifier.

The waveform level changes caused by an increase in the transmitted blanking level power output are shown by arrows in Fig. 27. The increase results in the blanking level of waveform A being more negative, a reduction in the amplitude of the negative control pulses at E, and a positive change in the modulator clamp reference potential. Considering a phase reversal in the modulator this causes a negative change in the blanking level at the input to the modulated amplifier, reducing its anode current and reducing the blanking level output power to off-set the original increase. The blanking level power output is therefore independent of any level change or low frequency interference introduced before the output sampling point, even if the change is introduced after the clamping point, that is, in the modulator or the modulated amplifier.

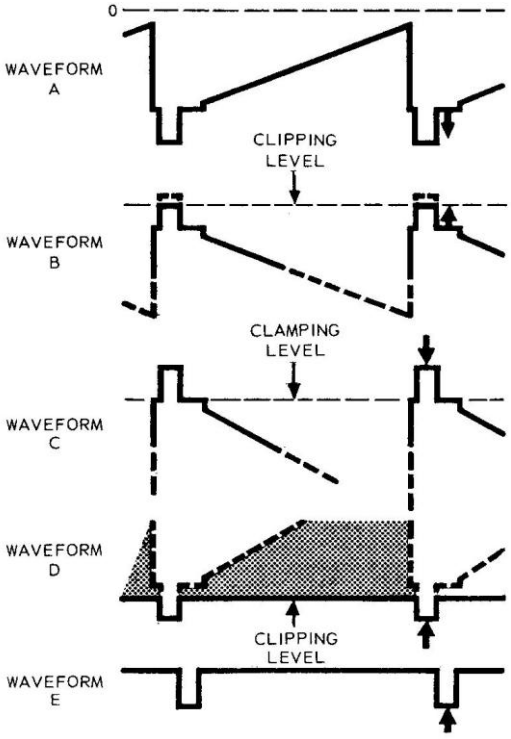


Fig. 27.

BLANKING LEVEL FEEDBACK WAVEFORMS.

4. PRACTICAL KEYED CLAMP CIRCUITS.

4.1 In a practical circuit, the clamp switch of the basic keyed clamp circuit in Section 3 is an electronic switch operated by clamp pulses. One feature that is desirable, but not achieved in some of the simple switch circuits, is that the clamp pulses should not be fed through the circuit to appear at the output. Many configurations of valves, transistors and diodes are possible, but this section deals with only three commonly used circuits; a two diode bridge circuit, a four diode bridge circuit and a single transistor circuit.

4.2 Two Diode Bridge Keyed Clamp. The circuit of a keyed clamp in which the switching is achieved by causing the conduction of two diodes is shown in Fig. 28. For convenience of drawing, the symbol for a semi-conductor diode is used, but high-vacuum diodes are very common, particularly in older circuits and in high level stages of transmitters. Fig. 28 shows that the clamp switch is essentially a Wheatstone bridge in which the clamp point of the circuit and the clamp reference potential are connected across opposite corners of the bridge and the clamp pulses are connected across the remaining opposite corners of the bridge. The diodes conduct during the short duration of the clamp pulses.

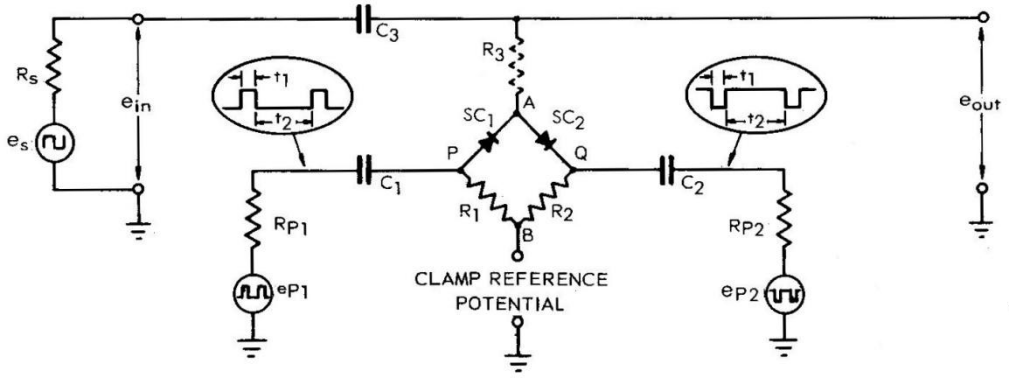


FIG. 28. TWO DIODE BRIDGE CLAMP.

Consider that the bridge section of the circuit is disconnected from the video signal circuit and the capacitor C3. During the clamping time (t1) the diodes conduct in series from the two clamp pulse sources in series, and an equal charge is built up on capacitors C1 and C2. Between pulses in time t2, the capacitors discharge through R1 and R2 respectively. The components SC1, C1, R1 form a peak rectifier clamp for the pulses e_{P1}, as do SC2, C2, R1 for the pulses e_{P2}. These two sets of pulses are then clamped to the potential that exists at point A. It is necessary, therefore, that the time constants C_1R_1 and C_2R_2 be long when compared with the clamp pulse spacing so that little discharge of the capacitors occurs during pulses. For television circuits typical values are:-

$$R1 = R2 = 0.1 \text{ to } 1M\Omega, \qquad C1 = C2 = 0.01 \text{ to } 0.1\mu F.$$

A conflicting requirement for these components is that there should be sufficient discharge of the capacitors C1 and C2 so that, during their charging time, a forward diode current as high as possible is maintained for the duration of the clamping time. This requirement also sets a lower limit for the time constant of the charge circuit of C1 and C2 (which is determined by the diode forward resistance and the clamp pulse source resistance) since if the charge is completed in the clamping time the diode current will fall to zero, and the switch will not be effectively operated. Because the clamp pulses have a very short duration and C1 and C2 have quite large values, the time constant for the charge of C1 and C2 in a practical circuit is many times the clamping time. The time constants C_1R_1 and C_2R_2 should also provide a recovery time for the peak rectifier clamp action, which will never allow diode conduction to be lost, because of a small drift of the clamp pulse amplitude which may occur in practice.

Because of diode resistance, the discharge of the capacitors between clamp pulses and the time constant of the charge circuit of the capacitors, the clamp pulses are not accurately clamped to point A. The two waveforms at points P and Q slightly overlap at their peaks when superimposed as shown in Fig. 29. This inaccurate peak rectifier clamping of the clamp pulses does not directly affect the accuracy of the final keyed clamping action.

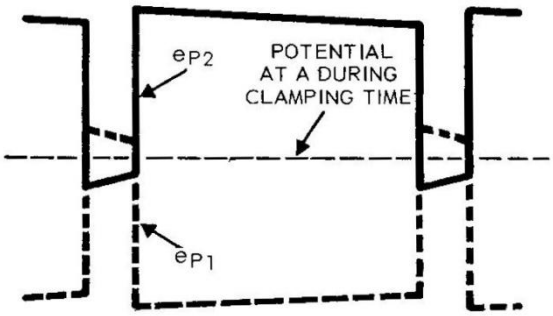


FIG. 29. CLAMP PULSE WAVEFORMS.

4.3 Since the peaks of the clamp pulses are clamped to the potential at A, between clamp pulses the polarities of the waveforms at P and Q with respect to A cause the diodes to be non-conducting. Therefore the diodes have disconnected point A from the rest of the bridge circuit giving the equivalent of an open clamp switch in the complete circuit.

When the values of R_1 and R_2, and C_1 and C_2 are equal, the diodes have equal forward resistances, and the clamp pulse amplitudes and source impedances are equal, the bridge circuit is completely balanced for both the clamping time, and the time between clamp pulses. With the diodes conducting during clamp pulses, the bridge circuit is completed and point A is at the same potential as point B. This gives the same effect as closing the clamp switch and connecting points A and B. When an error exists in the input blanking level, the series clamp capacitor (C_3) changes its charge so as to offset this error. The current through the capacitor divides equally between the two diodes of the bridge circuit, adding to the diode current in one and case, and subtracting from it in the other.

The unequal diode currents during error correction cause a slight difference of charge to be developed on C_1 and C_2, and a proportional change in the discharge currents of the capacitors during the following period between clamp pulses. However, because the values of C_1 and C_2 are much greater than the value of C_3, the charge during error correction is little different from that present when no error exists. The error correcting current through the diodes is returned to earth via the clamp pulse source resistance, therefore, the resistance of the clamp switch during the clamping time is the series parallel combination of the two diode resistances (R_f) and the two clamp pulse source resistance (R_p) as shown in Fig. 30. The values of R_1 and R_2 are large compared with the values of R_p and can be neglected.

As the conducting resistances of a diode decreases with increase in current, to obtain a low switch resistance, considerable diode current should be maintained for the duration of the clamping time as described in para. 4.2. This current should also be much larger than any clamping error correction current, to ensure diode current for the duration of the clamping time, and to permit stable operation of the circuit.

The time constant of the charge circuit of the clamp capacitor is determined by both the switch resistance and the video source resistance, and for fast error correction, the clamp pulse and video signal source resistances are made low. Both these resistances have values in the range between 200 and 4,000 ohms in practical circuits.

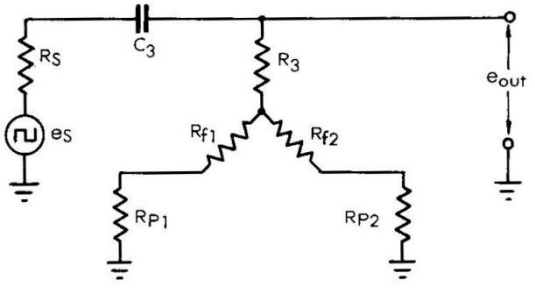


FIG. 30. CLAMP SWITCH RESISTANCE.

4.4 Waveform Amplitudes. It is necessary that the video signal should never cause the clamp diodes to conduct. Therefore, the clamp pulse waveform applied to the diodes between clamping times must exceed the peak amplitude of the video signal under any conditions. It is usual to make the peak-to-peak amplitude of the clamp pulses 2 to 3 times the peak-to-peak amplitude of the video signal. If the peak video signal amplitude exceeds the voltages at points P and Q between clamping times, one of the diodes will conduct via the low impedance path of the clamp pulse source, and, with C_3, behave as a peak rectifier clamp with a very long time constant. Consider a video signal as in Fig. 31a. With insufficient diode bias between clamp pulses, the peak white section of the waveform drives SC_2 into conduction, charges C_3, and clamps this peak to the potential present at Q. Because of the long time constant of the circuit, the capacitor charge is maintained and the remaining section of the line is shifted towards black (Fig. 31b). The signal is reclamped to the correct level during the back porch period, but is shifted again to the incorrect value by peak clamping of the next white section. The peak clamping causes a picture with a white section as in Fig. 31c to be reproduced with a dark streak to the right of white sections (Fig. 31d). The streak is completely removed by keyed clamping before the beginning of the next line and, therefore, does not appear to the left of the white section. This, and the fact that the long time constant of the circuit causes the streak to be of almost constant brightness, identifies this form of streaking from streaking caused by middle video frequency amplitude-frequency and phase-frequency distortion. Also, streaking because of amplitude and phase characteristics occurs at all signal levels and not only on signal peaks. As the blanking-to-white amplitude is greater than the blanking to sync. amplitude, peak rectifier clamping is more likely to occur on white signals than on sync. signals.

A similar streaking, but one which persists for many lines, is produced in A.C. coupled video amplifiers where excess video amplitude produces grid current which charges the coupling capacitor and gives peak rectifier clamping.

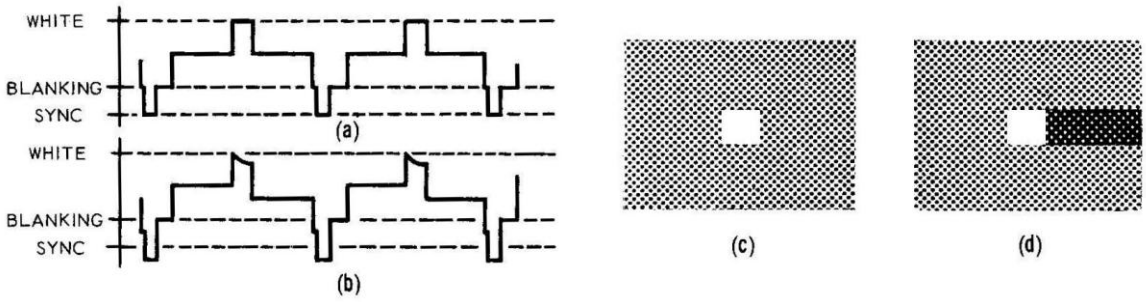


FIG. 31. EXCESS VIDEO SIGNAL AMPLITUDE.

4.5 Unbalance of Clamp Switch. With a balanced clamp switch, the video signal is clamped to the clamp reference potential, but if any of the impedances, or the clamp pulse amplitudes are varied, the level to which the video signal is clamped is varied also. Often the circuit is purposely unbalanced by varying the values of the resistors R_1 and R_2 of the bridge. This is usually achieved by connecting the clamp reference potential (which is commonly zero) to a potentiometer replacing R_1 and R_2 as in Fig. 32a. Resistors R_4 and R_5 limit the amount of unbalance possible so that the long time constants C_1R_1 and C_2R_2 are always maintained. Adjustment of the potentiometer allows the circuit to be corrected for small errors in clamp pulses amplitudes and for variations in the diode and source resistances. The unbalance also gives the circuit the advantage of being able to provide a clamp reference potential when the potentiometer is returned to earth.

The clamping potential when the switch bridge is unbalanced can be calculated by examining the circuit voltages and currents. Consider, that the bridge is balanced except for a variation of R_1 and R_2 and that no error correction is taking place. Also, to allow diode and source impedances to be neglected, assume that the time constants C_1R_1 and C_2R_2 are sufficiently long so that the clamp pulses with peak-to-peak amplitude of E_p are accurately clamped to the potential at point A.

During the discharge times of C_1 and C_2, the voltages in Fig. 32a at points P and Q with respect to the voltage at point A during the clamping time, are $-E_p$ and $+E_p$ respectively. Since the capacitors C_1 and C_2 charge in series, their charge currents are equal, and, for the circuit to be in a state of stable operation and not correcting an error, the discharge currents (I_D) through R_1 and R_2 must also be equal. Taking into account the polarity of the discharge current, P must be at a potential of $-I_DR_1$ with respect to B, and Q at $+I_DR_2$ with respect to B. The voltages and polarities in the bridge circuit are illustrated in Fig. 32b. Adding the voltages in the circuit gives the potential (E_A) at the clamping point A with respect to the clamp reference point B.

$$E_A = -I_DR_1 + E_p \text{ and } E_A = -I_DR_2 - E_p$$

Eliminating I_D and expressing E_A in terms of E_p, R_1 and R_2 gives:-

$$E_A = E_p \left(\frac{R_2 - R_1}{R_1 + R_2}\right)$$

Therefore, when the arm of the potentiometer is moved so that R_1 is made smaller in value, the clamping point moves positive with respect to any clamp reference potential. This can be estimated by remembering that point A is clamped to the potential at the balance pint of the bridge, which is the centre point of the potentiometer. Since the voltage between clamp pulses is negative at P and positive at Q, when the moving arm of the potentiometer is moved towards P the centre point of the potentiometer attains a proportion of the positive potential at Q and point A is clamped to this positive potential. Note that the clamp potential that is introduced by the unbalance of R_1 and R_2 can never be greater than the clamp pulse amplitude, and in practice is much less because of the presence of limiting resistors R_4 and R_5. Also, when R_1 and R_2 are not equal, a variation of the amplitude of the clamp pulses, even if both vary equally, will cause a variation of the clamping level. An important point is that the clamping level is determined by the currents in the circuit during the discharge time of C_1 and C_2, that is, between clamp pulses. By similar calculations the clamping potential can be found for other unbalanced conditions. When the bridge is balanced except for the amplitudes of e_{p1} and e_{p2} which have peak-to-peak values of E_{p1} and E_{p2} respectively:-

$$E_A = \frac{E_{p1} - E_{p2}}{2}$$

The clamping level can be varied by varying the clamp pulse amplitude, but the dependence of the circuit on clamp pulse amplitude is normally considered a disadvantage. The clamping level is relatively immune to variations of the forward resistance of the diodes and the pulse source resistance when these resistances are very small compared with R_1 and R_2 (<10% of t_1/t_2 R_1).

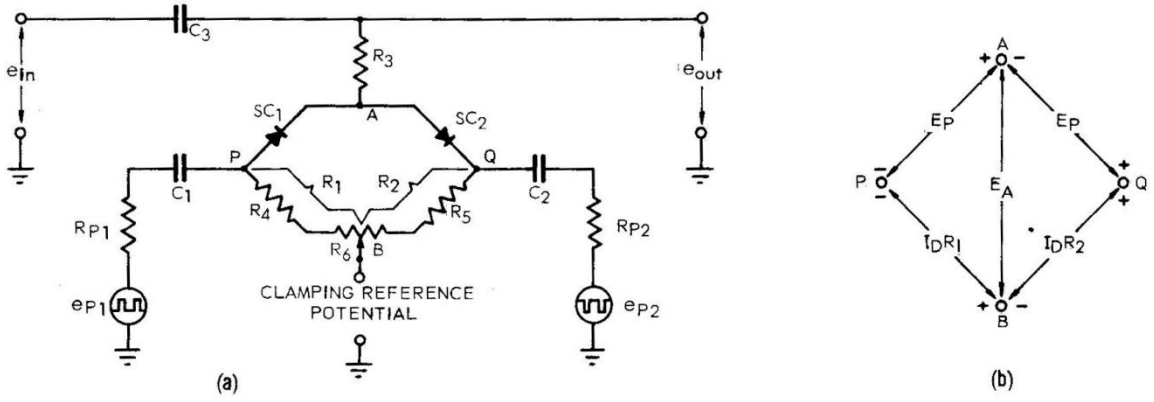
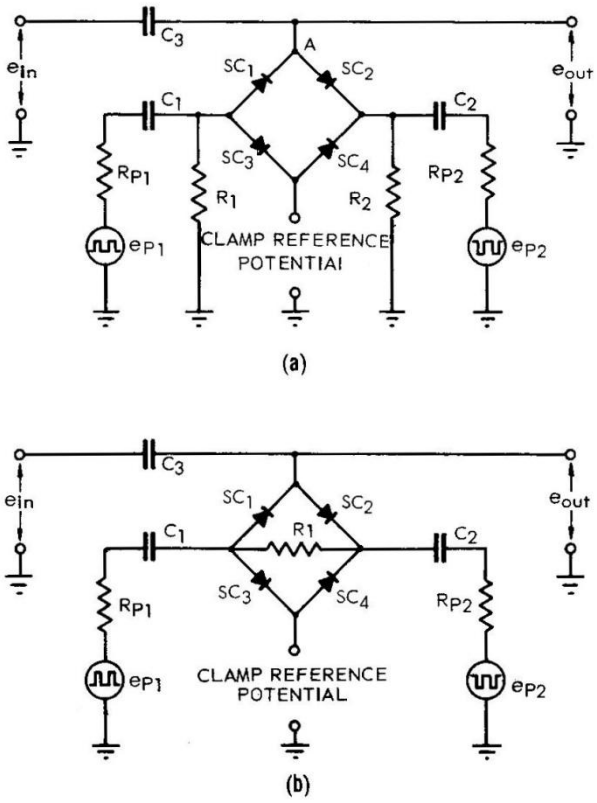


FIG. 32. UNBALANCE OF CLAMP SWITCH.

4.6 Four Diode Bridge Keyed Clamp. The dependence of the two diode bridge circuit on the clamp pulse amplitude is reduced practically to zero by adding two additional diodes to form the four diode bridge clamp in Fig. 33a. It is not necessary for the resistors R1 and R2 to be returned to the clamp reference potential (or to earth), and the circuit is often arranged as shown in Fig. 33b. Further, two clamp pulse sources are not essential and this allows the circuit to be modified as shown in Fig. 33c, where the clamp pulses are fed from a pulse transformer. All three forms of the circuit may be encountered.

The clamp pulses during the clamping time drive all four diodes into conduction and effectively connect the clamping point A to the clamp reference potential at B. The switch behaves as a low resistance, equivalent to the series parallel combination of the four conducting diodes and the two pulse source impedances. This is lower than the switch resistance in the two diode circuit. To make full use of the low switch resistance the clamp reference potential should be provided by a low impedance supply. The clamping error correcting current to charge the capacitor C3 divides between the two halves of the bridge, increasing the diode current caused by the clamp pulses in two arms and decreasing it in the other two arms.



During conduction of the diodes, the capacitors C1 and C2 in Fig. 33a are charged. The clamp pulses must have sufficient amplitude to prevent the video signal from causing diode conduction between clamping times, and thus producing streaking. The resistors R1 and R2 are provided to discharge C1 and C2 sufficiently between clamping times, so that adequate forward diode current occurs during the clamping time, and to maintain clamping in the presence of a small drift in the clamp pulse amplitude.

FIG. 33. FOUR DIODE BRIDGE KEYED CLAMP.

It is important in this circuit that the clamping level is obtained by the direct clamping of point A to point B through a low impedance path. In the two diode circuit the clamping level is indirectly from the discharge current through the resistors R1 and R2 between clamping times, and by the condition of balance of the bridge. The four diode circuit is only capable of clamping to the reference potential at B without the possibility of variation of the clamping level by unbalance, as in the two diode circuit. This is only strictly correct if the diodes have matched characteristics and the pulses are of equal amplitude, but a large unbalance of the circuit causes a change in clamping level of only a couple of percent of the clamp pulse amplitude. This is because the clamping level is established during the clamping time, when the voltage across the diodes of the bridge is only a small fraction of the clamp pulse peak-to-peak voltage.

To illustrate this, consider a four diode clamp circuit with diode forward resistances as in Fig. 34a, and clamp pulses of 30V p-p between points P and Q of the clamp switch. The values of the circuit resistances and capacitances are such that during the clamping time point P is +3V with respect to point Q, and 7V of the input clamp pulse is lost in the clamp pulse source resistance. The clamp pulse waveform between P and Q is shown in Fig. 34b. Between clamping times P is -40V with respect to Q so preventing diode conduction. Since $R_{f3} = R_{f4}$, the voltage between P and Q divides equally between the resistances and B is +1.5V with respect to Q. Also, because $R_{f2} = 2R_{f1}$ the voltage between P and Q divides so that A is +2V with respect to Q. Therefore A is 0.5V positive with respect to the clamp reference potential at B. The large unbalance in the diodes in the example has caused a clamping error of only 1% of the clamp pulse amplitude in this example. Changes in clamp pulse amplitude, when the four diode circuit is fed from two clamp pulse sources, produces clamping errors of a similar order.

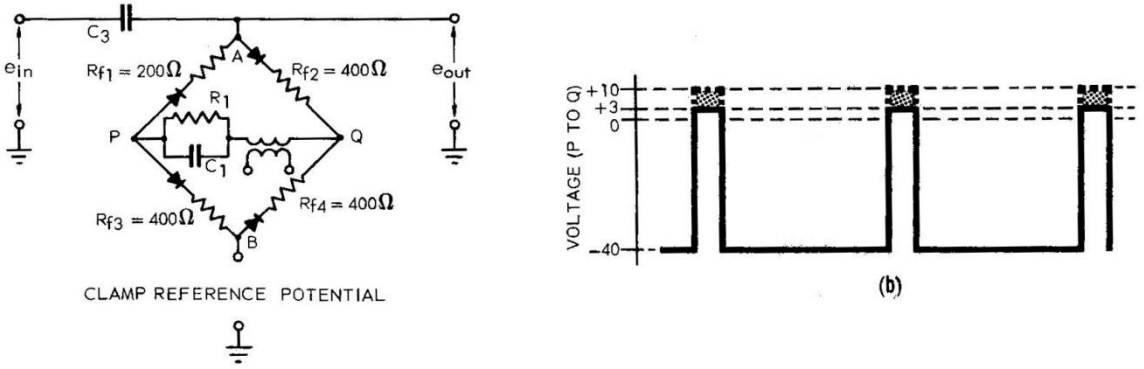


FIG. 34. UNBALANCED FOUR DIODE CLAMP CIRCUIT.

4.7 Clamp Pulse Break-through. Some transient clamp pulse break-through from the clamp pulse sources into the video circuit can occur in both the two diode and four diode circuits. It is usually caused by inequality in the timing or the shape of the two clamp pulse supplies, which will be modified by inequality of their amplitudes or source impedance, or because of unbalance of the capacitances of the non-conducting diodes. Remember that, when the circuit is correcting for an error in the clamping level, distortion of the waveform during the clamping period must occur as discussed in Section 3. Clamp pulse break-through is an additional degradation which is classified as synchronous noise, and it should be avoided.

It is not necessary that the clamp pulses have a rectangular shape, but it is essential that their shapes be the same. Consider that the two clamp pulse waveforms in Fig. 35 are applied to a two diode clamp circuit. One has been inverted so that they are conveniently superimposed for comparison. The diodes of the clamp switch conduct when the clamp pulse exceeds the clamping level that is established at the video output of the circuit. Therefore, from Fig. 35, e_{p1} causes diode S_{C1} to conduct before e_{p2} causes conduction of diode S_{C2}. For a short time between t_a and t_b the circuit is well out of balance, and the output waveform attempts to vary greatly from the correct clamping level. The effect is that "spikes" or "whiskers" are produced on the video waveform coincident with the transitions of the clamp pulses. The amplitude and duration of the spikes depends on the circuit component values and the waveform errors.

A pulse transformer is a nearly ideal source of clamp pulses for a keyed clamp circuit, since, with carefully constructed bifilar windings, identical pulse shape, amplitude and source impedance is possible.

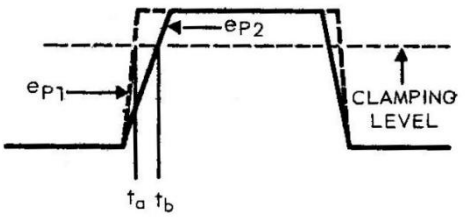


FIG. 35. CLAMP PULSE TIMING ERROR.

Unbalance of the circuit capacitances, particularly the capacitances of the diodes, also produces spikes on the waveform. There is little voltage across the diodes of the switch when they are conducting, but, at the end of the clamping time when the diodes cease to conduct, the clamp pulse waveform biases the diodes in the reverse direction by an amount approximately equal to the clamp pulse amplitudes. Each non-conducting diode behaves as a capacitance, and this capacitance must charge to the bias voltage. An equivalent circuit of the two diode bridge clamp used to examine the effect of capacitive unbalance is shown in Fig. 36a. Other components of the original circuit of Fig. 28 can be neglected. Neglecting temporarily the source resistance (R_S), and following clamping, the diode capacitance charge in series. When they are equal and the clamp pulse generator voltages and resistances are equal, the clamp pulse generators produce no signal at the output at point A. When the diode capacitances are not equal, unequal voltages are developed across them, and the potential at A changes exponentially to a value determined by the amount of circuit unbalance. Considering R_S, the circuit immediately following the clamping time is equivalent to a generator (e_A) producing an exponential change in the circuit of Fig. 36b. This circuit has the characteristics of a differentiating circuit with a time constant of a fraction of a microsecond in a practical circuit, and at the output "spikes" are produced following the switch off times of the diodes. At the commencement of the clamping time, the diode capacitance must discharge before the diodes can conduct. Unequal capacitances cause the voltages across the diodes to rise at different rates, and the diodes commence to conduct at different times, again producing spikes on the waveform. The preceding analysis assumes that the diode capacitances are constant, but, with semi-conductor diodes, the capacitance depends on the diode bias.

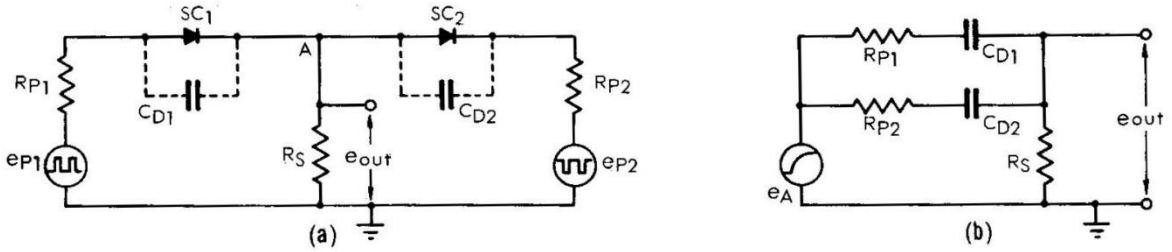


FIG. 36. UNBALANCEOF CLAMP CIRCUIT CAPACITANCE.

4.8 Single Transistor Keyed Clamp Circuit. A single transistor can be used to perform the function of the switch in the basic keyed clamp circuit. The circuit arrangement is as shown in Fig. 37 for an N-P-N transistor. Positive clamp pulses are applied to the base, and when the base is driven positive with respect to the emitter, current flows in the base-emitter circuit. The base-emitter junction and R1 and C1 behave as a peak rectifier clamp circuit, and clamp the positive extremes of the clamp pulses approximately to the reference potential at the emitter. In a specific example using a silicon N-P-N transistor and zero clamp reference potential, the positive extremes of the clamp pulses are established at approximately +0.6V because of the non-linearity of the base-emitter characteristics of the transistor which is shown in Fig. 38a.

The collector voltage of the transistor is supplied by the error in the voltage present at the clamping point A during the clamping time. It is possible for this error voltage to be either positive or negative, but the error introduced between clamp pulses is usually very small (approximately 10mV maximum for 1V p-p 50c/s sine wave interference). During the clamping time the collector voltage, therefore, is negative with respect to the base voltage and, for most practical error signals the collector-base junction, as well as the base-emitter junction, is forward biased.

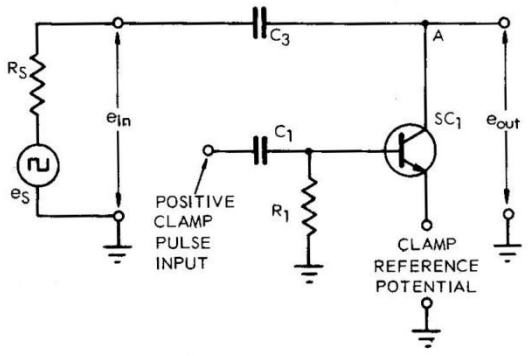


FIG. 37. SINGLE TRANSITOR KEYED CLAMP.

The low collector voltage section of the collector characteristic of a common emitter connected silicon transistor is shown in Fig. 38b. As the collector voltage is reduced, the collector current decreases slightly in approximately a linear manner until it reaches the "knee" and then it reduces rapidly to zero. The knee in the characteristic occurs at approximately 0.6V; this is caused by the change of the bias on the collector-base junction from the normal reverse bias to forward bias. The region of the characteristic at lower voltages than the knee is known as the saturation region, and the knee voltage is known as the saturation voltage. In the saturation region the collector current is practically independent of base current. The important characteristic of a transistor operating in the saturation region is that the collector-emitter circuit behaves as a very low resistance, typically of the order of 10Ω. The knee in the characteristic of a germanium transistor occurs at approximately 0.2V.

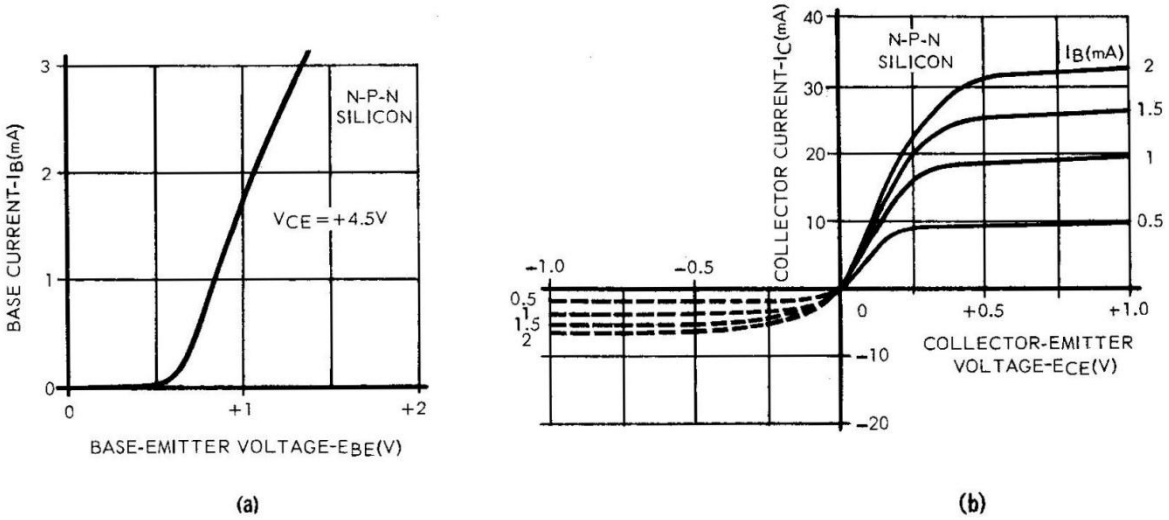


FIG. 38. TRANSISTOR CHARACTERISTICS.

A further characteristic of transistors is that the emitter and collector connections (or the polarity of the collector voltage supply) can be reversed and the transistor action will still exist. The practical limitation is mainly the consideration of power dissipation, but in addition the characteristics of the reversed transistor are usually changed from the normal characteristics. Some transistors are designed to be symmetrical. (Reversing the polarity of the supply to a transistor amplifier circuit can cause excess current which can damage the transistor). Because of the symmetrical nature of the transistor, the characteristic, which is normally confined to one quadrant of a graph, can be extended into the opposite quadrant as shown dotted in Fig. 38b, indicating the operation of the transistor under collector voltage conditions that are opposite to normal. The transistor is still operating in a saturation region for low values of reverse collector voltage. When the base bias current is supplied by a voltage (in this case by the clamp pulses) applied between base and emitter independent of the collector voltage polarity, the emitter current does not reverse its direction until the reverse collector current exceeds the base current.

The transistor used as a clamp switch is always operated under saturation conditions and is driven "on" (into conduction) by the clamp pulses. Under these conditions, for small positive or negative error voltages, the transistor behaves as a very low resistance, and the charge time constant for the correction of the error signal is determined mainly by the source resistance.

Between clamping times the base is driven negative with respect to the emitter and the junction. Therefore, is reversed biased. The transistor is cut-off, no collector current flows, and the video signal present on the collector is not affected. The video signal must not be of sufficient amplitude to allow the collector-base junction to be forward biassed between clamp pulses, or peak rectifier type clamping will occur on video peaks, as with the two and four diode bridge circuits.

When the transistor keyed clamp circuit or any other type of keyed clamp circuit is followed by a transistor amplifier, the amplifier input stage must be designed to present a high impedance to the output of the clamp circuit. So that extremely high input impedances are not required, the value of the clamp capacitor can be increased to maintain adequate line tilt. A typical value is 0.1µF. This introduces a requirement for very low video signal source resistance and clamp switch resistance if the clamp circuit is to be fast acting.

4.9 Clamp Pulse Generators. To this stage we have considered clamping occurring in the back porch period. It would be sufficient for horizontal blanking periods that clamping pulses reoccur at line rate, and be delayed say 6µS after the horizontal synchronizing time. The leading edges of the sync. pulses or "horizontal drive" pulses from a sync. pulse generator could be used to trigger the clamp pulse generator. ("Horizontal drive" pulses are distributed to provide horizontal synchronising information particularly in studio installations where non-composite video signals are encountered). This is satisfactory for non-composite video signals. However, when we examine the clamping times required during the vertical blanking period this scheme is not satisfactory for composite video signals.

Fig. 39a illustrates the equalizing pulse and broad pulse section of the vertical blanking period. Here horizontal synchronizing information is conveyed by the leading edges of the pulses at twice line frequency, but 6µS after the leading edge of a broad pulse the video signal is still at sync. level. To ensure that the clamp pulses occur when the video signal is at blanking level, it is necessary that the clamp pulse generators be "slaved" to the video signal to be clamped, and arranged so that the clamp pulse generation is initiated by the trailing edges of all pulses. If the clamp pulses are delayed 1µS after the trailing edges of all horizontal synchronizing, equalizing and broad pulses, as shown in Fig. 39b, they will always occur at a time when the video signal is at blanking level. They will, however, occur at irregular intervals at approximately twice line rate during the vertical sync. period.

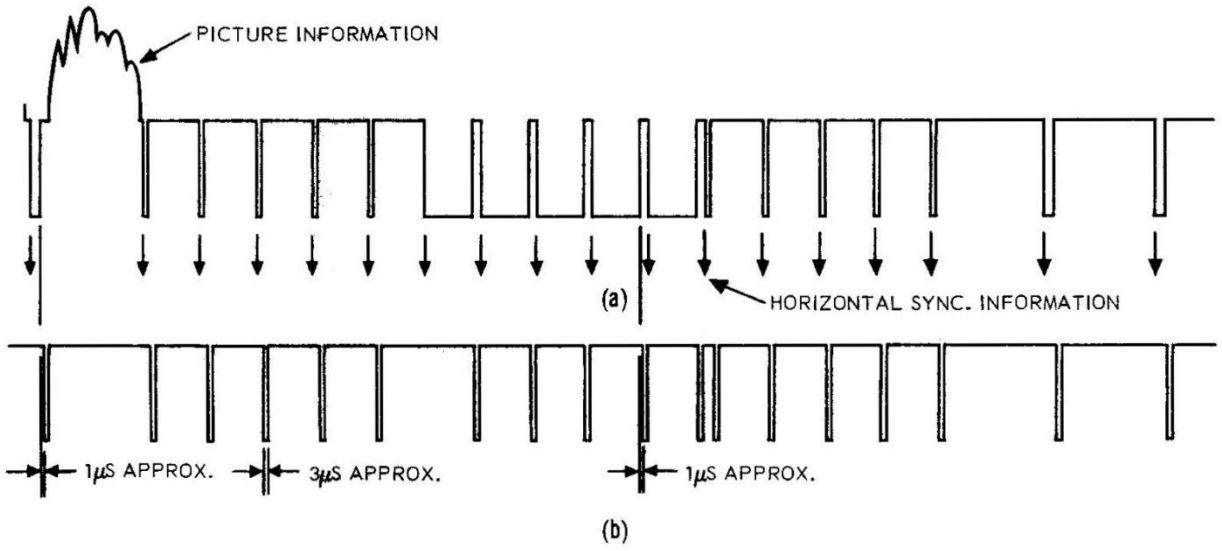


FIG. 39. CLAMP PULSES DURING VERTICAL BLANKING PERIOD.

4.10 A block schematic of a system for clamp pulse generation is shown in Fig. 40a. Only an outline of the operation is considered. The detailed operation of each block is considered in other papers of the course. The video signal is fed into a sync. separator and the synchronizing information removed for the composite video signal. A section of the waveform at A, for simplicity containing only horizontal sync. pulses, is shown by waveform A in Fig. 40b. The sync. pulse waveform is passed through a differentiating circuit and the output is waveform B. The differentiated pulses are fed into an amplifying and clipping stage. Here waveform B is inverted and then clipped so that only the section shown by waveform C remains. This has approximately squared up the "spikes" form the differentiating circuit.

Waveform C is differentiated and the resulting negative "spikes" clipped off to produce waveform D which is passed into a pulse shaping circuit. This is a multivibrator circuit designed so that when waveform D is below level E_A, the output (waveform E) has a voltage E_B, and when waveform D is above level E_A, waveform E has a voltage E_C. The output is a series of clamp pulses. The phase splitter provides the two sets of opposite polarity pulses required for some circuits. The duration of the pulses can be varied within a limited range by varying the switching level E_A of the pulse shaping circuit, thus varying the switching times of the circuit. Varying the time constant of the first differentiating circuit varies the delay between the trailing edges of the sync. pulses, and the leading edges of the clamp pulses.

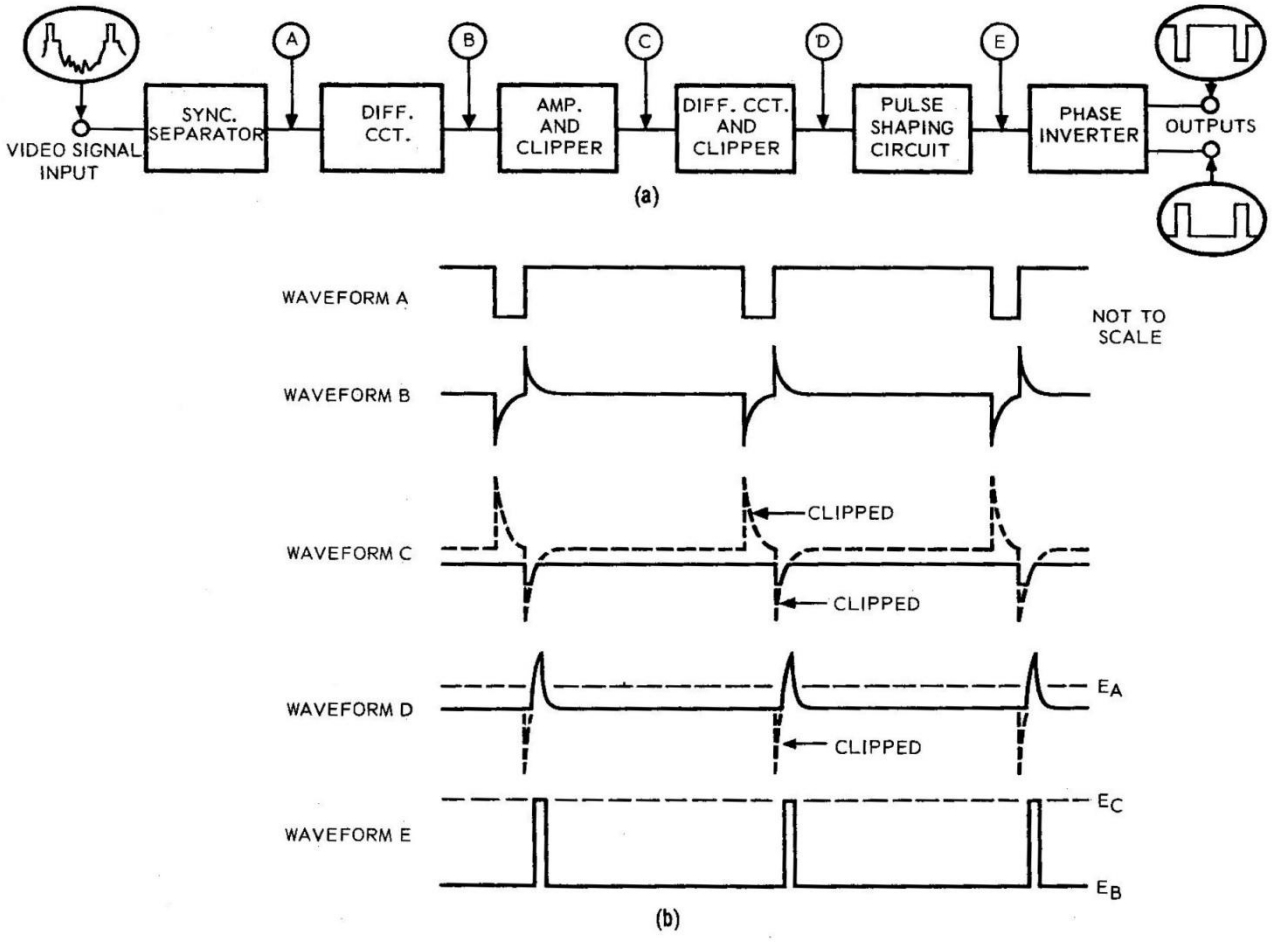


FIG. 40. CLAMP PULSE GENERATOR.

4.11 Another method of developing correctly timed clamp pulses uses a "delay line". A "delay line" is an artificial transmission line, usually having lumped inductance and capacitance, designed so that large amounts of signal delay are achieved in a small physical space. The velocity of propagation per unit length along the line is much less than along normal transmission lines. The details of transmission lines and "delay lines" are considered in other papers of the course.

The important properties of delay lines for the generation of clamp pulses, are the delay of the signal introduced by the line and the reflection of the signal when the line is not correctly terminated in its characteristic impedance. When a delay line is shorted at its terminating end, a signal voltage reaching the end is reflected after undergoing a phase reversal, and is propagated back towards the input. If the source impedance matches the characteristic impedance of the line, no further reflection occurs.

A block schematic of a system for generating clamp pulses using a delay line is shown in Fig. 41a. The sync. pulses are separated from the rest of the video signal in the sync. separator. The output of the sync. separator (waveform A) is illustrated in Fig. 41b. The sync. separator output impedance is designed to match the characteristic impedance of the delay line. The sync. pulses travel down the line, and at B the incident signal is delayed by 0.5µS as illustrated by waveform B_I. The wave continues down the line, and at the short circuit termination is reflected after undergoing a reversal of voltage. The wave takes 2µS to travel from B to the termination and back to B, and, with negligible loss in the line, the reflected signal at B (waveform B_R) is an inverted and delayed replica of B_I. The reflected signal continues to the input, and is completely absorbed by the correctly terminated input.

The output from the delay line tap at B (waveform B_T) is the algebraic sum of the waveforms B_I and B_R. This waveform has the negative pulses removed by a clipper, and the output from the circuit (waveform C) is a series of clamp pulses delayed 0.5µS from the trailing edges of all pulses, and with durations of 2µS. These pulses always occur when the composite video signal is at blanking level. Clamp pulses cannot be produced with durations greater than the duration of the preceding input pulse, or greater than the duration of the vertical sync. serrations. A phase inverter would be included in the circuit if required.

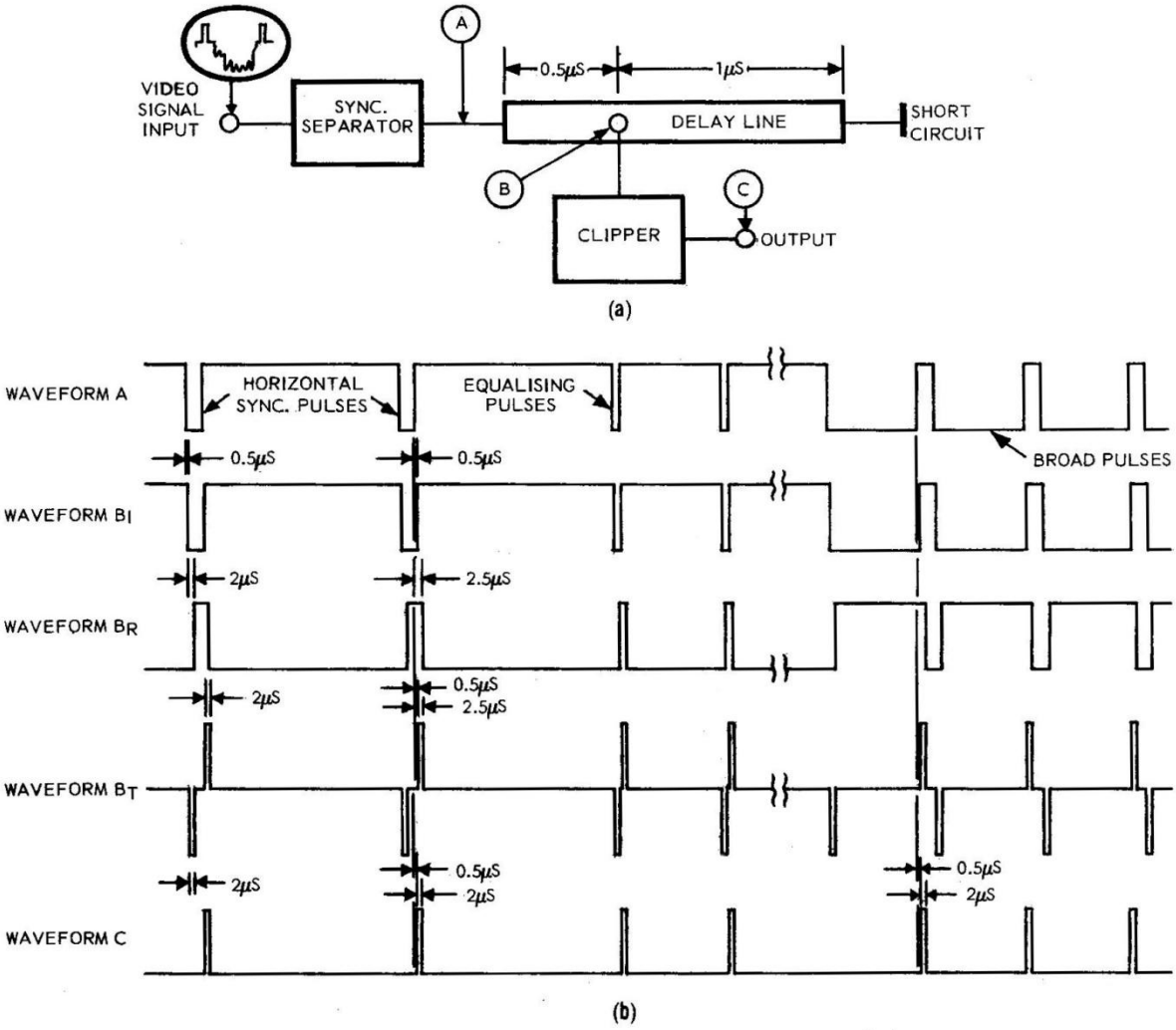


FIG. 41. DELAY LINE CLAMP PULSE GENERATOR.

4.12 The most common phase inverter used in conjunction with clamp pulse generators is the split load phase inverter as shown in Figs. 42a and b. However, any type of phase inverter could be used. The circuits in Fig. 42 are at their best when negative clamp pulses are applied to the inputs, and these cut-off the valve or transistor during the clamping times. For a P-N-P transistor circuit, positive clamp pulses would be required at the input. When the circuit is cut-off the outputs are completely isolated, and the output impedance of each pulse source is equal to the respective load resistances of the phase inverter circuit. If the input pulses to the phase inverter are of opposite polarity so that the valve or transistor is conducting during the clamping times, loading of one output is reflected to the other output. Also the output resistance depends both on the load resistors, and the valve and transistor resistances.

In some cases, particularly when very low values of clamp pulse generator impedances are required, a pulse transformer is inserted in the output of the pulse generator, and two secondary windings give outputs with opposite polarities. For accuracy of pulse amplitude and output resistance, the secondaries are often bifilar wound.

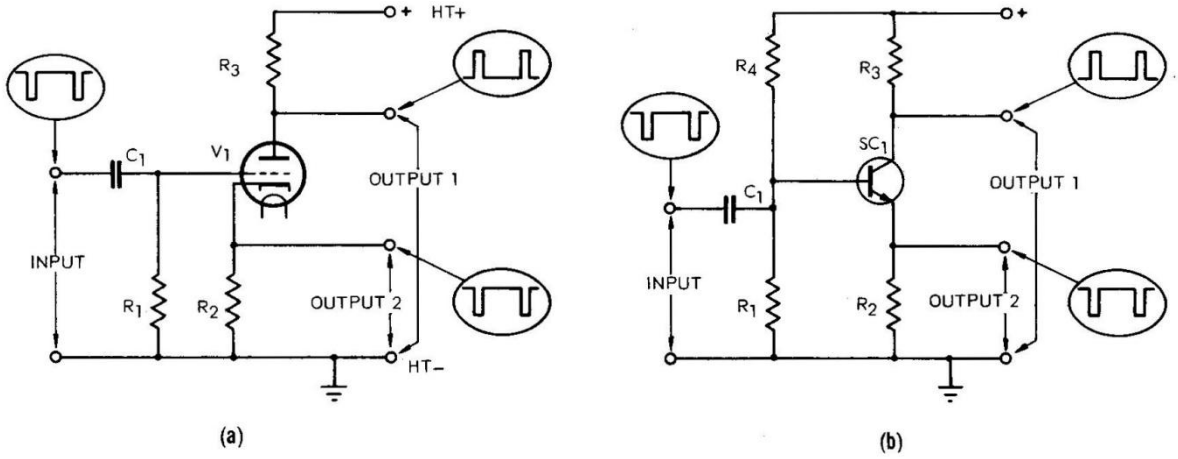


FIG. 42. PHASE INVERTER CIRCUITS.

4.13 Clamping of a composite video signal is not always carried out during the back porch period. In some practical applications clamping is achieved at sync. pulse tips. This is often used when degradation of the back porch is to be avoided, and also is commonly used when the picture signal is to be clipped from the sync. pulses. It has the further advantage that no special clamp pulse generator is required. The sync. pulse information is extracted from the composite video signal and amplified to drive the clamp circuit. Removal of the picture signal is not essential, as long as the keying signal is always of sufficient amplitude to maintain the clamp switch diodes non-conducting between clamping times.

Non-composite video signal at studio installations are commonly clamped in the period where sync. pulses will later be inserted. After sync. pulses have been added, these are clipped at the correct level and any degradation caused by clamping is also removed. The clamp pulses for non-composite video signals cannot be derived from the video signal since no synchronizing information is present. The clamp pulses are usually derived from horizontal drive but sync. pulses from an external source could also be used.

5. *TEST QUESTIONS.*

1. *Draw peak rectifier clamp circuits that will clamp the negative extreme of a waveform to (i) 0V (ii) +20V.*

2. *Describe the operation of a positive peak rectifier clamp considering zero source resistance.*

3. *How is the operation of a peak rectifier clamp affected by:-*
   (i) Source resistance;
   (ii) Batteries of each polarity inserted separately at both X and Y in Fig. 43a;

4. *(i) Draw the output waveforms obtained from the circuit in Fig. 43a for each of the following conditions when C=0.1μF, R_1 = 0.1MΩ and the source voltage is a 1kc/s square wave of 20V p-p:-*

   (a) R_S = 0, R_f = 0; (b) R_S = 800Ω, R_f = 0;
   (c) R_S = 0, R_f = 200Ω; (d) R_S = 800Ω, R_f = 200Ω.

   (ii) Indicate on the waveform obtained in (i), the time constants of the various sections.
   (iii) What would be the output waveform if the input signal contained a D.C. component of +30V?

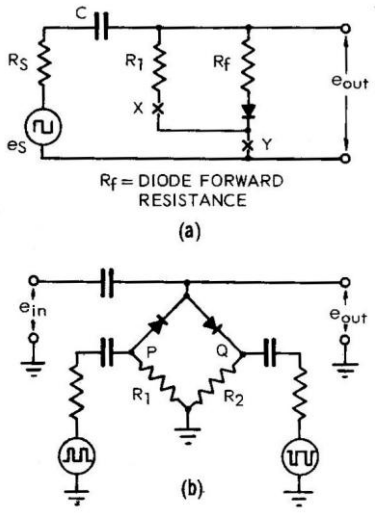


FIG. 43.
TEST QUESTION CIRCUITS.

5. *(i) Calculate the "average" amplitudes of the sections of the output waveforms from the circuit of Fig. 43a when C = 0.1μF, R_1 = 0.1MΩ, R_S = 800Ω, R_f = 200Ω and the source voltage is a series of (a) positive pulses; (b) negative pulses of 9V p-p with durations of 5μS and pulse spacings of 67.5 μS.*
   (ii) Do the actual output waveforms vary far from the waveforms showing the "average" amplitudes of each section? (Consider the tilt introduced onto waveforms).

6. *(i) Estimate the output waveforms from the peak rectifier clamp in Fig. 43a for a source voltage that is a series of positive rectangular pulses with amplitudes of 15V p-p, durations of 10μS and pulse spacings of 110μS. Consider that C is large enough so that negligible discharge occurs between clamping times and that R_S = 4kΩ, R_1 = 100kΩ and R_f = 1kΩ.*
   (ii) Repeat the problem in (i) for R_1 = 1MΩ, and compare the output amplitudes.

7. *Explain the principle of a basic keyed clamp circuit and state the advantages of the circuit compared with the peak rectifier clamp.*

8. *A keyed clamp circuit is fed from a source resistance of 800Ω and contains a series capacitance of 1,000 pF and a clamp switch with a resistance of 200Ω. The error in the level of the signal to be clamped is 0.1V immediately before the clamping time which has a duration of 2.3μS. Draw the output waveform from the circuit before, during and after the clamping time, and indicate amplitudes and time constants.*

9. *A video signal has superimposed on it a 1V p-p sine wave interfering signal of 1302c/s. The video signal is clamped during the back porch period at 64μS intervals and the clamping times are of negligible duration. Estimate the approximate output interfering signal if (a) all, (b) only 50%, of the blanking level error is removed in each clamping time.*

10. *Describe the operation of a blanking level stabilising system using feedback techniques.*

11. *Describe the operation of a electronic switch used in a keyed clamp circuit.*

12. *A two diode clamp switch as in Fig. 43b is balanced except that R_1 is 0.4MΩ and R_2 is 0.6MΩ. To what levels would the video signal output from the circuit be clamped if the clamp pulses and P and Q have amplitudes of (i) 15V p-p; (ii) 10V p-p?*

13. *Draw waveforms to show the timing of suitable clamp pulses during the vertical blanking period of a composite video signal, and describe with the aid of a black diagram how these clamp pulses could be generated.*

END OF PAPER.